Identification and Analysis of Parasitic Depletion Mode Leakage in a Memory Select Transistor

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Introduction

Low yield was reported for a non-volatile embedded memory array. This memory array is constructed of cells with two transistors per cell. The cell is comprised of a non-volatile transistor in series with a special n-channel (select) transistor. This select transistor is comprised of n+ with an LDD (Lightly-Doped Drain) spacer on the source side and a DDD (Doubly Diffused Drain) n+ junction on the drain side. In one case, this n-channel transistor was observed to exhibit single bit OFF leakage in a 32K array. In another case, there was general leakage (many cells in the array) observed between drain junctions of neighboring transistors, even though these were isolated by field oxide. The objective of the failure analysis described in this paper was to characterize the electrical behavior of the leakage and determine the exact location and cause of the leakage.

Sample Identification

Appropriate dice for analysis were determined based on wafersort rejects and extensive memory pattern write and read operations on the Credence memory test platform (Model BTMA2001). The details of the electrical analysis on the Credence are beyond the scope of this paper. Leakage measurements were performed on the suspected select transistor by direct memory access of the leaky cell. The leakage current by the direct memory access technique was compared to the leakage current measurement obtained after physical isolation of the leaky cell with the FIB (Focused Ion Beam).

Traditional Approach

Selected dice were exercised on the Credence tester in programming mode to help generate enough photons for effective emission microscopy. Location(s) of the leakage was identified on the Emission Microscopy System (FA1000) with a 50X objective, but the resolution of the image was not enough to provide localized information within the failing cell. Leakage measurement with direct memory access lacked the control required to isolate the electrical behavior of the leakage source further. Deprocessing of the sample down to bare silicon did not reveal any defects or abnormalities in the cell(s) in question. We were forced by circumstances to try new techniques.

New Approach

Direct contact and control of the terminals of the select transistor(s) under investigation was obtained by polishing the samples down to the contact plugs (removal of metal 1 from the array was necessary to lay down FIB traces). The FIB was used to make contact with the DDD n+ junctions, select transistor gate and LDD-N+ source junction. The FIB also provided micropads for microprobing to obtain the I-V behavior of the leakage.

Microprobing of the select transistor drain to source leakage (case #1) and select transistor drain-neighbor select transistor drain leakage (case #2) both exhibited a depletion mode (JFET) like I-V behavior suggesting presence of shallow n-type dopant impurities in the path of the leakage.

Determining the exact location of the leakage source within the cell(s) in question was obtained by combining the microprobing and photoemission techniques. To obtain higher magnification, a metallurgical microscope (Zeiss Axiotron) was utilized in conjunction with the photoemission camera and modified microprobes. A spatial resolution on the order of three hundred nanometers was achieved and thus helped to identify the exact location of the leakage source.

Case #1 Select Leakage

Several dice were identified with the bitline leakage problem in the memory cell. Figure 1 shows schematically the path across the select transistor. Emission microscopy was used in conjunction with decoding to identify the exact location of the failing cell as shown in figures 2 and 3. The failing cell creates a leakage on the bitline, which can be eliminated by programming the failing cell. Once programmed, the leakage is gone due to the fact that the NVM (Non Volatile Memory) transistor is in series with the select transistor. This electrical information points to the select transistor as the source of the leakage. A test mode known as DMA

(Direct Memory Access) was used to measure the leakage current at the failing cell. Leakage on the order of 18 μA was found at 1.4 volts applied between the source line and bitline. Note: The cell is unprogrammed for this measurement.

The identified failure was deprocessed by stripping to substrate with HF and staining with Wright etch to delineate the junctions.[1] No anomalies were observed as seen in figure 4. Another die was prepared in a similar fashion as above except Sirtl etch was used as the final delineation step.[2] No stress related or dislocation related anomalies were observed with the failing cell.

The next step was to eliminate any possible gate involvement associated with the word line over the failing cell using Passive Voltage Contrast (PVC).[3] PVC uses the electron beam of a conventional SEM to charge the surface at low accelerating energies to an equilibrium level. Any conductors, which have a path to ground, will not charge to equilibrium and appear bright. The sensitivity of measurement for the technique typically extends into the femtoamp range and is dependent on the beam current as well as scan area/scan time. No gate related leakage was observed.

The DMA current was recorded at 18.9 μA on another select failure and analyzed further. The part was surface polished to remove metal 2 and metal 1, leaving behind the tungsten plugs. Laser marks were placed equidistant from the failing cell to simplify navigation and the FIB (Focused Ion Beam) was used to connect the source line, drain and word line to allow the leakage behavior to be characterized. Figure 5 shows the location of the deposited platinum traces and probe points. The drain contact was created to allow direct electrical access to the select transistor. Figure 6 is a family of curves generated by stepping the Vgs (gate to source voltage) negative in 0.5 volt increments with a vertical scale of 5 μA/div. The curve at Vgs=0.0 with 1.4 volts drain force is 18 to 19 μA. This data point matches the previously measured DMA value of 18.9 μA prior to deprocessing. Note the depletion mode behavior of the transistor with a pinchoff of –4 volts. Figure 7 is the family of curves obtained for positive gate drive values from 0 to 1.5 volts in 0.5 volt steps and 10 μA/div. The saturated depletion mode characteristic transitions to an enhancement mode characteristic.

In order to perform emission microscopy with adequate spatial resolution the sample needs to be planar with minimal refracting oxide and under a high numeric aperture lens. The FIB preparation was done on the sample with all the metal interlayer dielectric removed by surface lapping. This allowed greatly improved spatial resolution of the poly word lines. A temporary probe station to take advantage of this was put together using an aluminum plate and 3 vacuum probes as shown in figure 8. The probe tips were configured on a low entry angle as shown in figure 9 to allow biasing of the select transistor. Figure 10 clearly shows the location of the photoemission on the poly wordline associated with the left edge of the select. The drain to substrate breakdown was checked and found to be normal. The exact depletion site was triangulated with a sized overlay to the drawn layers. Dopant concentration control by modifying masking layers resulted in elimination of the problem in subsequent lots of silicon.

Case #2 Drain to Drain Leakage

Similar analytical methods were used to identify and analyze the drain to drain leakage. Extensive test patterns were used to pin down the relationship of the leakage path. The failure pattern was a “bull’s-eye” pattern on the wafer. Figure 11 shows schematically the drain to drain leakage across a field oxide isolation. A long integration photoemission image (1-hour) taken during programming revealed a leakage along the memory row in figure 12. Note the diminishing leakage away from the cell being programmed. As was done in case study 1, FIB probe points (figure 13) were created directly to the adjacent drain regions. Figure 14 is a curve of the leakage between adjacent drain structures that revealed a depletion characteristic of 30 μA at 4 volts. To confirm the series nature of the leakage, probing was performed on each side of a drain structure. The curve of the leakage in series across an isolated drain structure gave a depletion mode characteristic of 13 μA at 4 volts as shown in figure 15. Photoemission performed with an AC bias revealed the location of the leakage as shown in figure 16. DC bias will generate one or the other of the two sites based on polarity. A failing die from the center of the wafer was decorated using the Wright etch and compared to an edge die which was passing the electrical tests. No differences or anomalies to explain the failure were observed (Figure 17). Note: The drain area is labeled “D”.

Additional analysis was performed to map the nature of the depleted region by using Scanning Capacitance Microscopy.[4] This technique allows dopant concentration as well as polarity to be mapped on a properly prepared sample. In order to prepare the sample it is first stripped to substrate using 49% HF. The sample is then swabbed lightly with blue colloidal silica and a cotton swab. Organic soap and a foam swab are then used to clean the surface. The sample is baked at 200C for 5 minutes and exposed to 254nm UV light prior to the scan to dissipate surface charge. Figure 18 is a capacitive scan from the edge of the wafer corresponding to a good die. Figures 19 and 20 are capacitive scans from the center of the wafer corresponding to a bad die. Note the n-type-depleted slot crossing the p-

type region associated with every other row. The Wright etched sample from figure 17 was examined with the AFM in 3D topographical mode as seen in figure 21. The Wright etch enhanced defect stands a mere 50 angstroms in height but is visible and corresponds in location to the capacitive scan.

Corrective Action

The first case study involved dopant concentration optimization at the drain of the select transistor by modifying mask layers and good results were obtained in subsequent lots of silicon.

The second case study also involved a cell layout change to remove a parasitic n-type implantation from the FOX isolation region

Summary

Two elusive leakage problems were identified, analyzed and eliminated from the process using multiple analytical techniques. The FIB was used to make electrical contact to drain regions, which lacked a contact for microprobing. Once the electrical parameters were obtained, photoemission analysis was performed with modified probes for higher spatial resolution to pinpoint the leakage path. Finally, scanning capacitance microscopy methods were used to prove the presence of the n-type depletion path.

The theory of a parasitic n-type dopant creating leakage was based on the I-V curves for the select transistor in the first case. In the second case the sample was stripped down to bare silicon with HF 49% and a high-resolution capacitance probe technique was used to image the silicon surface. Very clear and positive confirmation of the presence of the parasitic n-type dopant was confirmed.

Acknowledgments

Cuong Trinh and Lucas Wong from the technology development group for suggestions and experimental results on the two case studies.

References

1. Margaret Wright Jenkins, “A new preferential etch for defects in silicon crystals,” Journal of the Electrochemical Society, vol. 131(5), pp. 757-762,1977.

2. Thomas W. Lee,”A Review of Wet Etch Formulas for Silicon Semiconductor Failure Analysis”, Microelectronic Failure Analysis Desk Reference, Fourth Edition, EDFAS ASM. P. 598.

3. Jim Colvin, ”A New Technique to Rapidly Identify Gate Oxide Leakage in Field Effect Semiconductors Using a Scanning Electron Microscope”, Proceedings of the International Symposium for Testing and Failure Analysis, (Los Angeles, CA), October 1990, pp. 331-336.

4. Y. Strausser, J. Colvin,”Atomic Force Microscopy: Modes and Analytical Techniques with the Scanning Probe Microscope”, Microelectronics Failure Analysis Desk Reference, Fourth Edition, EDFAS ASM. Pp. 337-339.

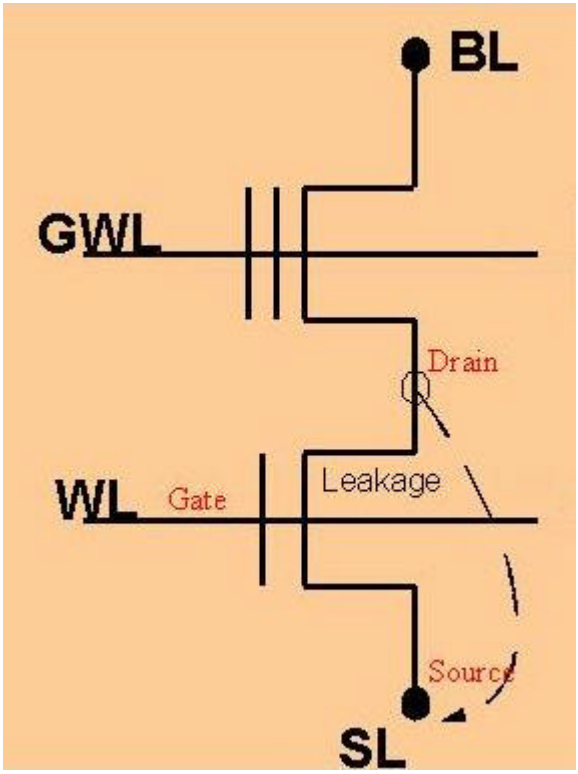

Figure 1 Schematic view identifying the leakage path across the select transistor.

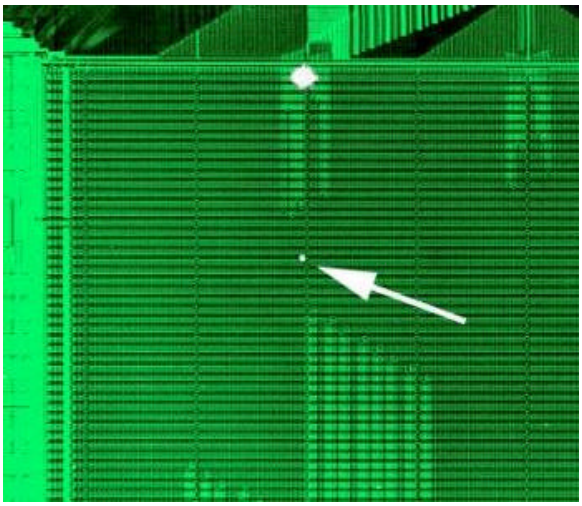

Figure 2 Emission image of the failing cell during program of word line 00 (Bright spot above). The failing cell leaks during program sufficiently to be detected.

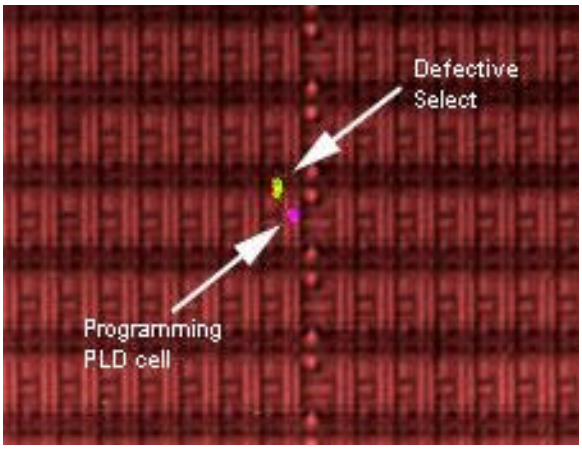

Figure 3 Close up emission image of the failing cell during program of word line 00 (Defective select). During programming the expected emission is shown adjacent to the select failure.

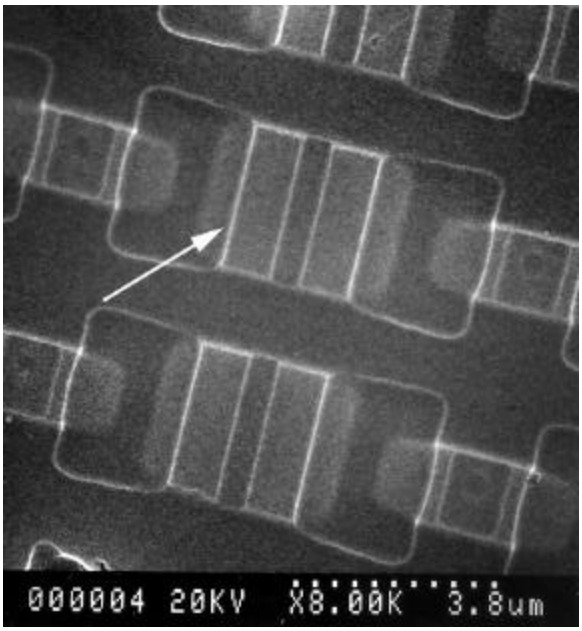

Figure 4 SEM view of the failing cell after Wright etch enhancement. No defects were observed.

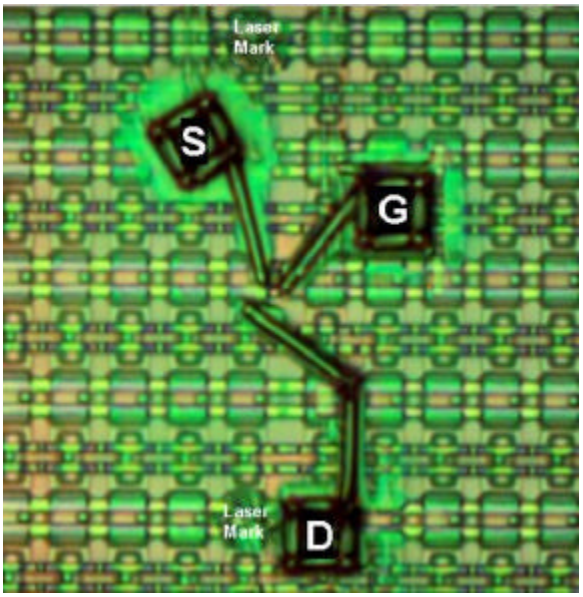

Figure 5 Optical image of the region after FIB connection. The pads allow probing of the defective select transistor to obtain a family of curves as well as emission information.

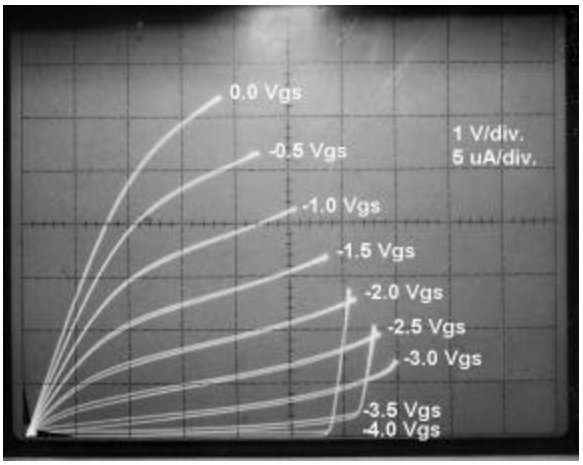

Figure 6 Family of curves for gate voltage values from 0 volts to –4 volts. Note the depletion style behavior of the transistor.

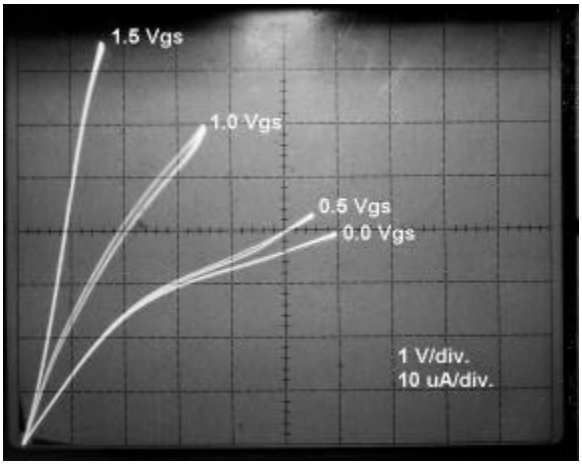

Figure 7 Family of curves for positive values of Vgs. The transistor acts as a saturated depletion in parallel with the expected enhancement characteristics.

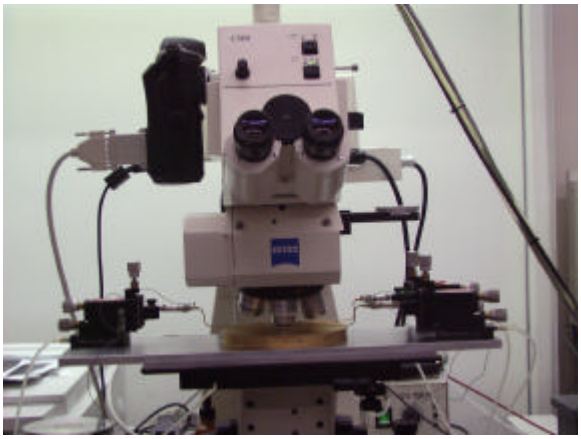

Figure 8 Setup necessary to allow probing in conjunction with emission microscopy at high spatial resolution.

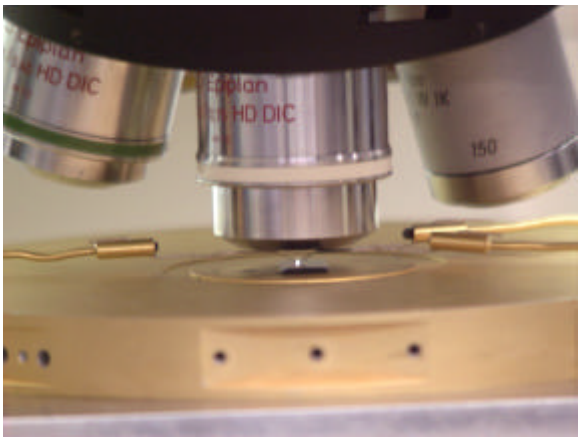

Figure 9 Close up view of the setup used to probe with emission. The objective used is .75NA 100X.

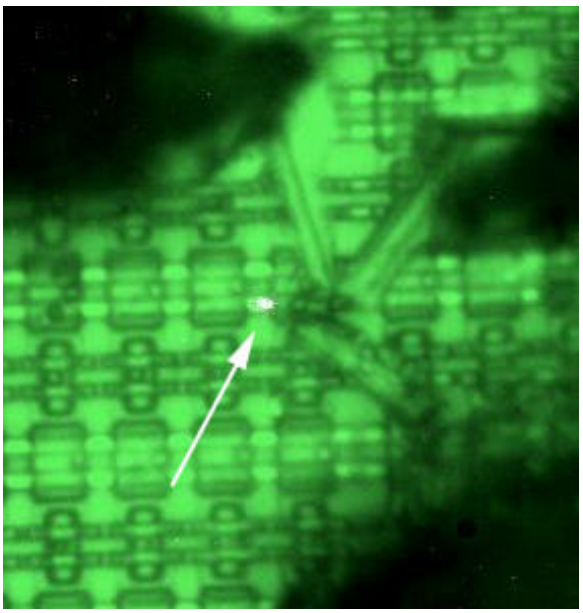

Figure 10 Photoemission image of select leakage with 6 volts drain to source and 0 volts gate to source.

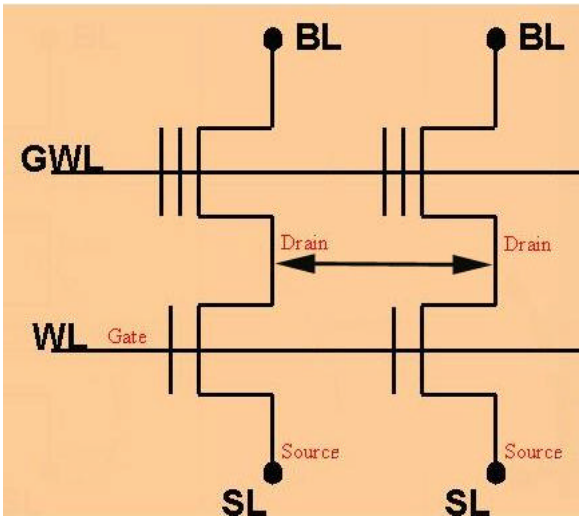

Figure 11 Schematic view identifying the leakage path across adjacent drain regions.

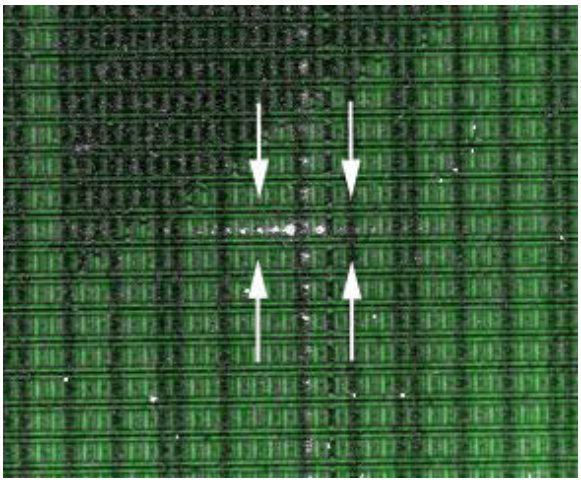

Figure 12 Photoemission image of the adjacent drain leakage during programming. Note the diminishing leakage away from the cell being programmed.

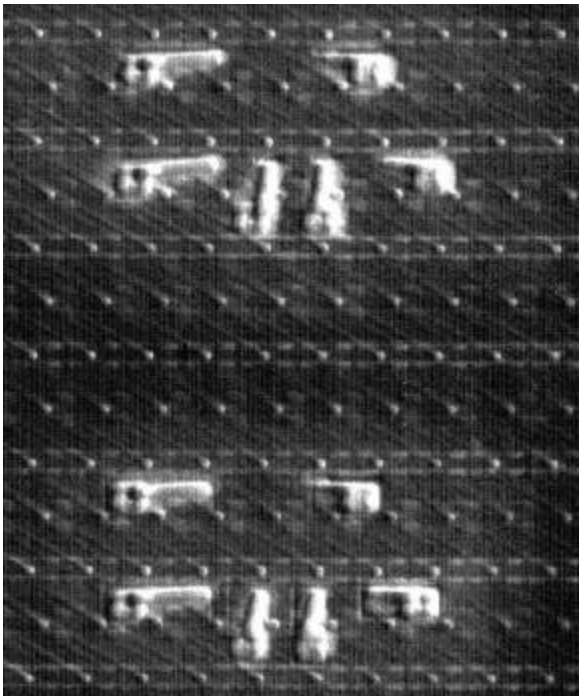

Figure 13 FIB deposited probe points for adjacent drain leakage measurements.

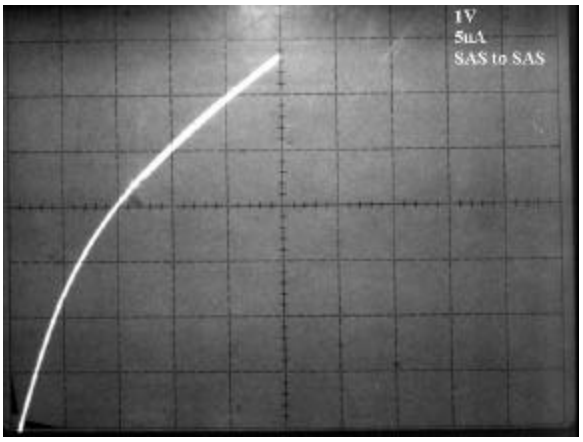

Figure 14 Curve of the leakage between adjacent drain structures. Depletion characteristic of 30 μA at 4 volts.

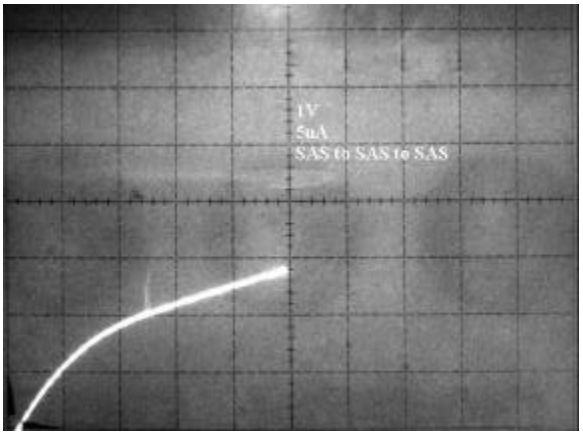

Figure 15 Curve of the leakage in series across an isolated drain structure. Depletion characteristic of 13 μA at 4 volts.

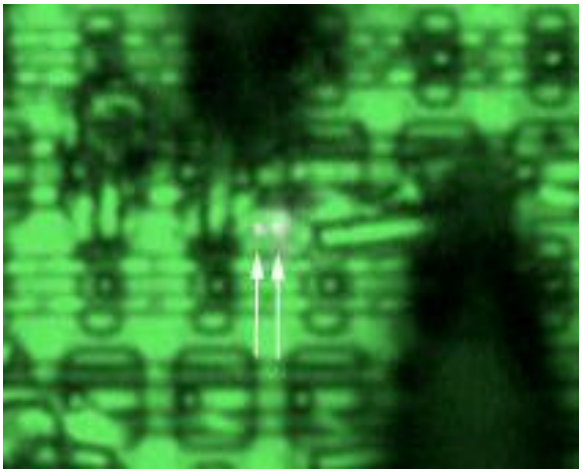

Figure 16 Photoemission image of the adjacent drain leakage with ac bias applied via the probe pads. DC bias will generate one or the other site based on polarity.

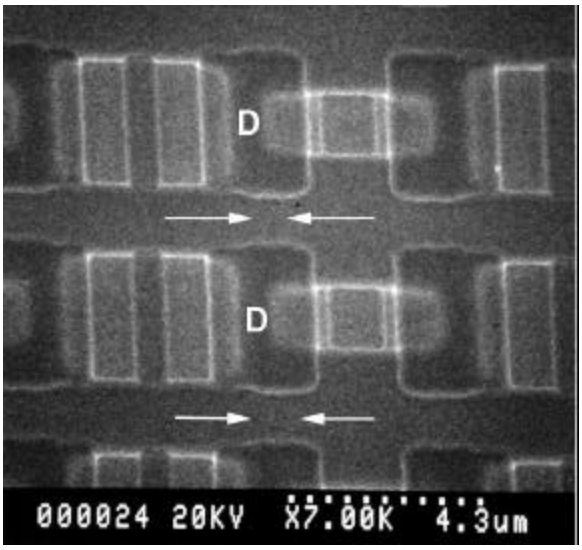

Figure 17 SEM photo of the adjacent drain leakage after Wright etch enhancement. No defects were observed. Note: Orientation is 90 degrees from the previous images.

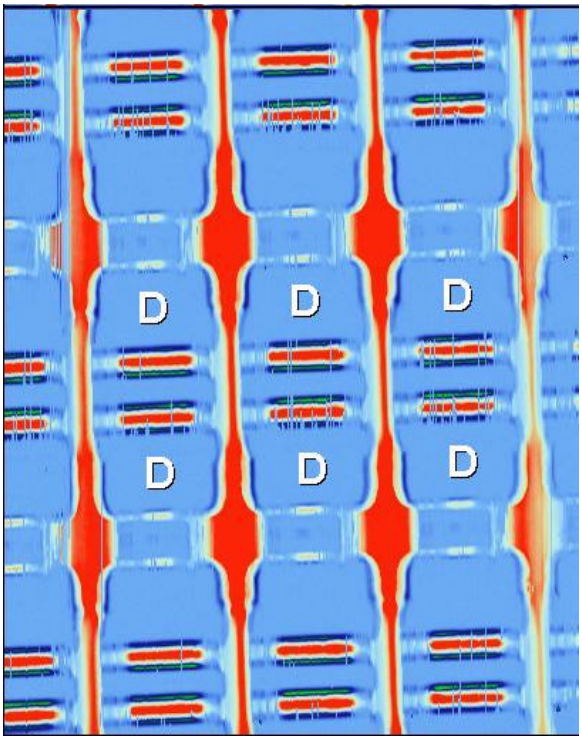

Figure 18 Capacitance probe image of a normal die at the edge of the wafer. Note that the light blue region indicates n+ type and dark blue indicates n– type dopants. The red regions are the p– areas.

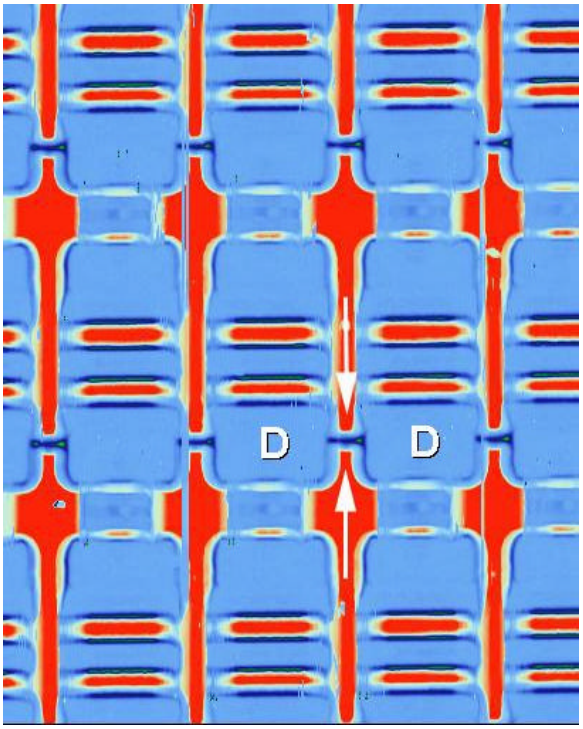

Figure 19 Capacitance probe image of a failing die due to adjacent drain leakage from the center of the wafer. The arrows illustrate one of 8 leakage paths across. Note that the light blue region indicates n+ type and dark blue indicates n– type dopants. The red regions are the p– areas.

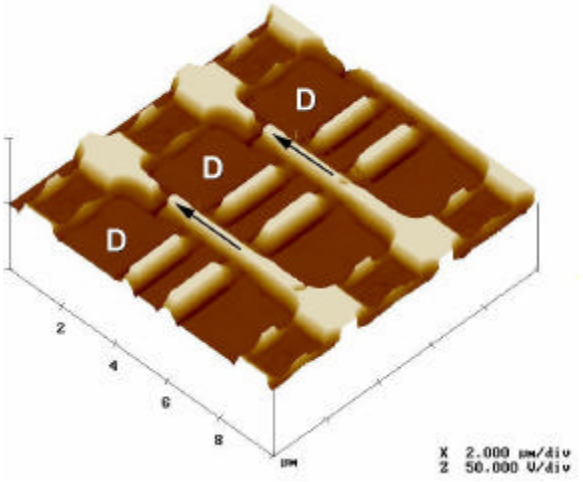

Figure 20 Capacitance probe image from figure 19 displayed in 3D format.

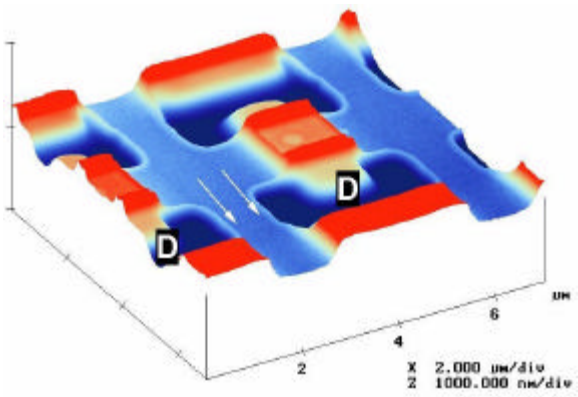

Figure 21 3D AFM topographical image of the area from figure 17. The Wright etch enhanced defect stands a mere 50 angstroms in height.