# THE IDENTIFICATION OF COMPROMISED OXIDE INTERFACES USING NOISE SIGNATURE TECHNIQUES FROM A CONSTANT CURRENT SOURCE

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## Abstract

Fabricated gate oxide defects are one of several mechanisms that can result in abnormal $I_{CC}$ standby current values and/or functional failures within a device. A new method to identify compromised oxide interfaces is called oxide noise signature analysis (ONS). This method allows rapid electrical identification of compromised oxide associated with a failing device using a constant current source to bias the device, either in an $I_{CC}$ standby mode, or by biasing directly a suspect pin. The resulting voltage on that pin is used to measure oxide stability as a result of the constant current source.[1] If this voltage manifests itself as impulse noise "Impulse noise is characterized by long quiet intervals followed by bursts of high amplitude noise pulses."[2], then this noise is a signature that there is, somewhere on the device, a compromised oxide interface. ONS is an electrical signature which indicates the existence of visible photon emission from the defect, regardless of overlying geometry. The success of Emission Microscopy is dependent on the overlying geometry which can interfere with photon detection. ONS methods are quite valuable to augment IDDQ testing methods as well as Failure Analysis and Wafer Level Reliability (WLR).

**DAMAGED OXIDES,** which have not been electrically overstressed, act as spark gaps. When a "wounded" oxide is biased with a constant current, impulse noise results. By band limiting and amplifying the resulting applied bias associated with the DUT (Device Under Test) the presence or absence of impulse noise is easily determined. In this paper, the theory of operation of the ONS circuit will be discussed as well as interpretation of various ONS signals. Fabricated gate oxide integrity defects, transient induced defects, and metal/oxide/metal interface failures identified by ONS will be discussed on a case by case basis. These types of defects can result in abnormal $I_{CC}$ standby current values and/or functional failures with the device in addition to the ONS signature. Emission Microscopy[3] and Passive Voltage Contrast[4] (PVC) will be used to complete the analysis of failures identified with the ONS signature. Latent ESD (LESD) damage on input pins creating a walking wounded phenomenon have been analyzed with ONS principles from previous work.[5] These types of defects have latency associated with them that can result in subsequent failure. The work in this paper will focus on how to incorporate ONS testing for rapid identification of compromised oxide interfaces, sometimes even with devices that exhibit normal Icc Standby or IDDQ values.
Finally, the implementation of ONS for Wafer Level and package level testing will be discussed.

## The Oxide Noise Signature Circuit

**Theory of Operation.** Refer to the block diagram in Figure 1. The circuit consists of a voltage controlled constant current source which is used to drive a constant current across the DUT. The resulting voltage drop across the DUT is buffered at J2 and supplied to a lowpass filter. The lowpass filter supplies the DC value of the DUT bias to a summing circuit which adds the negative desired set-point of the DUT (Compliance voltage set-point) to the actual measured DUT bias. The result is multiplied by -2.7 and used to control the dependent current source such that Vcc is maintained on the DUT. The signal at J2 is also supplied to a high gain active filter for detection of the ONS signal.

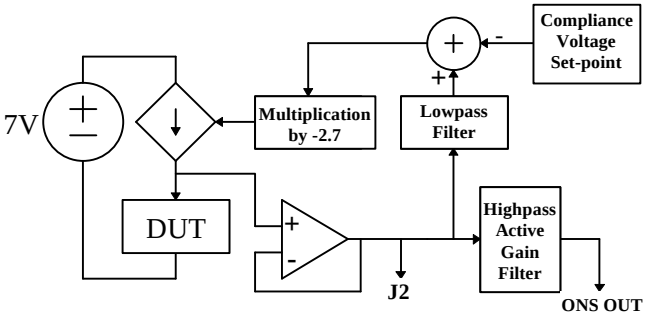



**Figure 1** Block diagram of the ONS circuit.

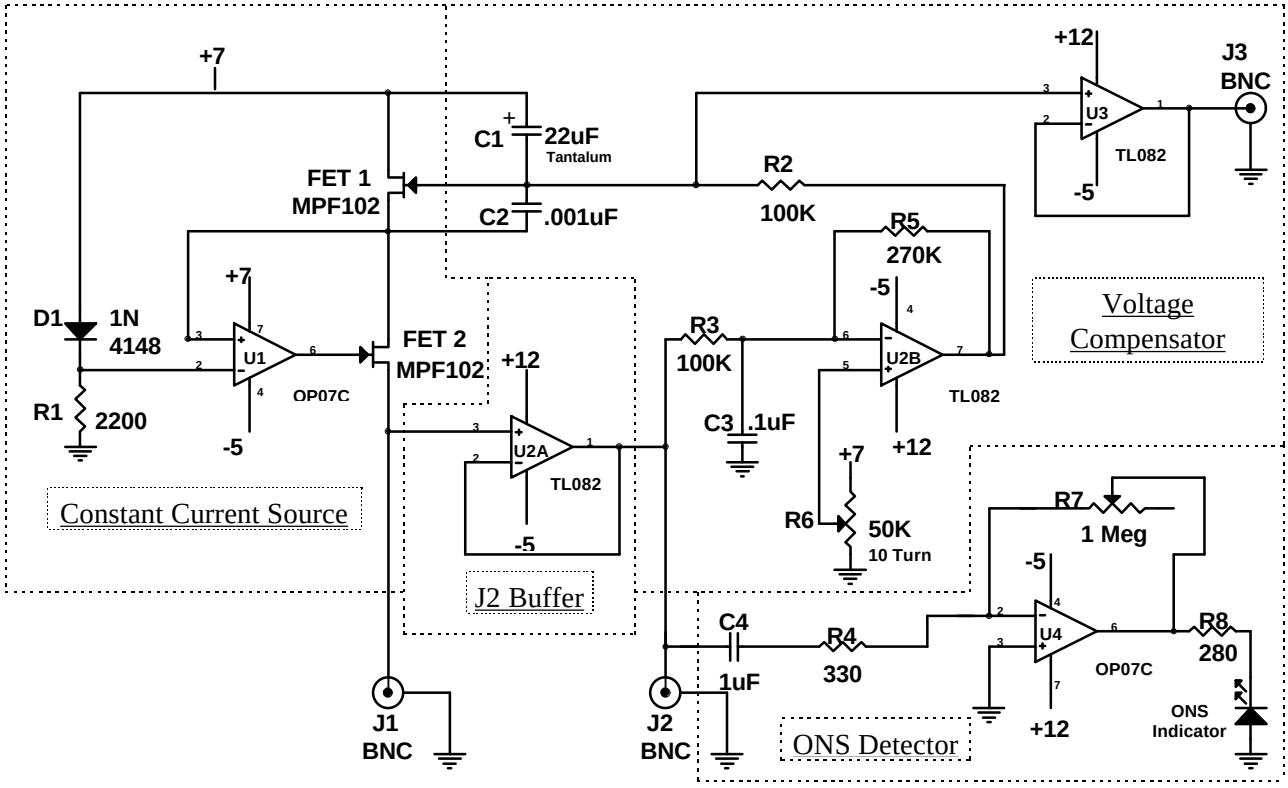



**Figure 2** Schematic diagram of the voltage compensating constant current source for oxide noise detection.

Figure 2 contains the schematic diagram for the ONS circuit with the parts list following. The circuit operates as follows: Operational amplifier U1 has a maximum offset sensitivity of 100 uV and in conjunction with FET 1, FET 2, C2, R1, and D1 comprise the precision constant current portion of the circuit. The inverting input of U1 is biased .7 volts below Vcc by D1 and R1 and remains constant regardless of device load. U1 is used as a comparator to maintain a constant voltage drop across FET 1 by controlling the gate bias of FET 2. Negative feedback is achieved through use of the + input of U1 since FET 2 is an n-channel transistor connected in an inverting configuration. C2 is used as a stabilization capacitor for U1. FET 1 is configured as a load resistor. The constant current set-point is adjusted by changing Vgs on FET 1. If Vgs is increased on FET 1, the voltage drop Vds on FET 1 will begin to decrease from .7 volts. The + input of U1 will increase causing FET 2 to increase conduction reestablishing equilibrium. The source of FET 2 is supplied to the DUT by shielded connector J1. The maximum response of the constant current source is 3000 to 6000 Hz depending on parasitic capacitance.

U2A is a BiFET Operational amplifier follower selected for its high input impedance characteristics of $10^{12}$ ohms. The high impedance is necessary since the current source has a range of 7 mA down to 900 pA. The buffered output from U2A is supplied to connector J2 for monitoring the voltage applied to the device under test (DUT).

The output of U2A is also supplied to R3 and C3 of the voltage compensator circuit. R3 and C3 make up a lowpass prefilter for U2B. U2B is configured with a gain of: -R5/R3 = -270K/100K = -2.7. The desired Vcc set-point at the DUT is controlled by potentiometer R6. The output of U2B drives RC combination R2 and C1 connected to the gate of FET 1 allowing the constant current source to be adjusted with a delay approximately equivalent to:

$R2*C1/gain_{U2B}$ = 100E3*22E-6/2.7 = 0.8 seconds until Vcc is achieved.

Operational amplifier U3 is a BiFET high impedance follower which allows the Vgs of FET 1 to be measured externally at connector J3. J3 correlates to the set-point of the constant current source and therefore provides a reading as to the average Icc supplied to the DUT.

Operational amplifier U4 has a 100 uV offset voltage specification and in conjunction with C4, R4, R7, R8, and a LED comprise the ONS detector circuit. C4, R4 and R7 on U2 create an active high pass filter with the cutoff frequency not less than:

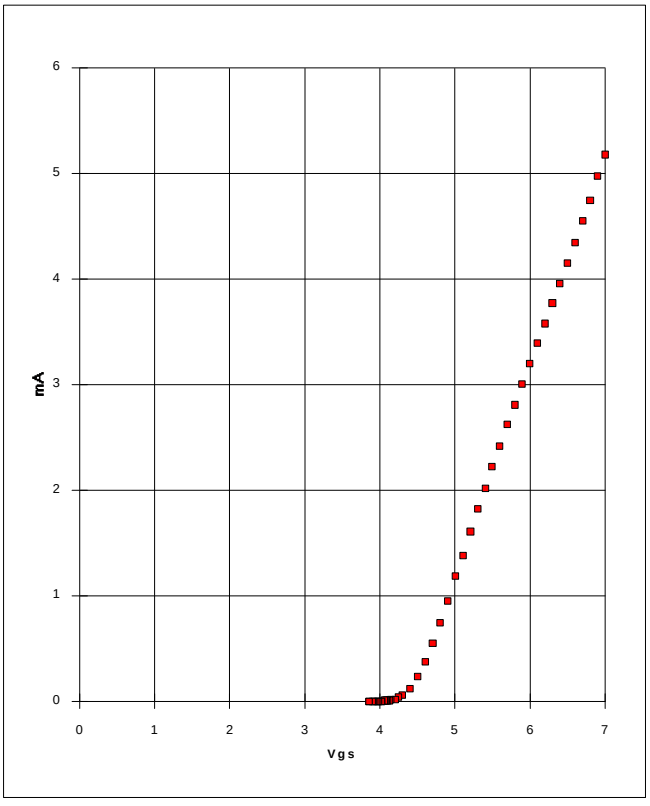
1/(R4*C4) = 1/(330*1E-6) = 3030 Hz. The active filter gain is adjustable with R7 and has a maximum gain of:
-R7/R4 = 1E6/330 = 3030. By amplifying the band limited impulse noise, (remember the maximum response of the constant current source is 3000 to 6000 Hz depending on parasitic capacitance) discrete events of impulse noise are easily seen at the LED driven by U4 across dropping resistor R8. The LED will flash each time an impulse occurs in this frequency range. Stray 60 Hz AC signals are heavily attenuated with this configuration to minimize or eliminate shielding requirements.

**Parts List.** D1 = 1N4148, R1 = 2.2KΩ, U1 = TIOP07C, U2A and U2B = TL082, U3=TL082, U4 = OP07C, FET 1 and FET 2 = MPF102 depletion JFET, J1-J3 = BNC chassis mount connector, C1 = 22 uF tantalum, C2 = .001 uF, R2 = 100kΩ, R3 = 100KΩ, C3 = .1uF, C4 = 1 uF, R4 = 330Ω, R5 = 270KΩ, R6 = 50KΩ (10 turn potentiometer), R7 = 1MΩ potentiometer (1 turn), R8 = 220Ω, ONS Indicator = AlAs high bright LED with lens, PC board (General purpose etched), and an aluminum chassis box. All resistors are 1/4 watt metal film.

**Shielding, Circuit Layout and Power Supplies.** Stray AC fields will not adversely affect the ONS circuit due to the high attenuation below 600-1000 Hz of the detector, however, the following steps are recommended. Use low capacitance shielded cables between FET 2 and the DUT (RG59 cable) to minimize the stray AC noise components. Use a pre-etched multipurpose PC board or etch your own. Use 8 pin dip sockets for U1-U4 for diagnostic purposes. Keep lead lengths short, no more than 1 inch for the constant current source section of the circuit. Use an aluminum box to house the circuit and ground the box only to the DUT to avoid potential groundloops. Use regulated power supplies for the ONS circuit. Following these tips will ensure a stable subnanoamp current source for ONS as well as other applications.

**Circuit Calibration.** Since connector J3 correlates to the set-point of the constant current source, a lookup table of Vgs (Gate to source voltage) to the constant current set-point (Constant current at the DUT) values can be created for IDDQ measurement purposes. Note: This calibration is unnecessary for ONS detection purposes. The values in Table 1 and Graph 1 were obtained with the +7 V fixed supply set at 7.38 volts in this case. To obtain a calibrated table of lookup values, connect a calibrated DVM (Digital Volt Meter) to J3. Connect a calibrated Digital Ammeter to connector J1 such that J1 drives the ammeter short. Disconnect pins 7 and 5 of U2B and jumper the R6 control directly to the gate of FET 1. This allows the current set-point to be directly controlled with R6. Start at 7 volts and reduce the voltage in increments as shown in Table 1. Record the Icc at each voltage until 1 uA is reached. Obtain the remaining values by connecting 10 MΩ of impedance across J1 without the ammeter and set R6 so J2 = 5 volts. The constant current is now 5/10MΩ = 500 nA. Reduce Vgs until 4 volts is at J2 and Icc is now 400 nA and so on. Finish with 100 MΩ of resistance across J1 and a foil shield for the low to sub nanoamp range. Note that the voltage across the load (DUT) must range from 0.2 to 6.68 volts for stability in this current range.

The lookup table can be implemented with an analog to digital converter for direct readout and logging of IDDQ values if desired.




**Graph 1. Plot of constant current at J1 vs Vgs at FET 1 from table 1.**

**Table 1. Numeric values of the gate to source voltage at FET 1 vs the constant current drive at connector J1.**

| Vgs (Volts) | Current (Amps) | ** | Vgs (Volts) | Current (Amps) | ** | Vgs (Volts) | Current (Amps) |
|---|---|---|---|---|---|---|---|
| 7 | 5.18mA | * | 5.5 | 2.22mA | * | 4.15 | 13.1uA |
| 6.9 | 4.97mA | * | 5.4 | 2.02mA | * | 4.13 | 10.2uA |
| 6.8 | 4.75mA | * | 5.3 | 1.82mA | * | 4.1 | 7.2uA |
| 6.7 | 4.55mA | * | 5.2 | 1.60mA | * | 4.09 | 6.2uA |
| 6.6 | 4.35mA | * | 5.1 | 1.39mA | * | 4.07 | 4.7uA |
| 6.5 | 4.15mA | * | 5 | 1.19mA | * | 4.05 | 3.3uA |
| 6.4 | 3.96mA | * | 4.9 | 955uA | * | 4.03 | 2.4uA |
| 6.3 | 3.77mA | * | 4.8 | 748uA | * | 4.01 | 1.7uA |
| 6.2 | 3.58mA | * | 4.7 | 555uA | * | 3.99 | 1.1uA |
| 6.1 | 3.39mA | * | 4.6 | 378uA | * | 3.97 | 700nA |
| 6 | 3.20mA | * | 4.5 | 234uA | * | 3.95 | 500nA |
| 5.9 | 3.00mA | * | 4.4 | 123uA | * | 3.93 | 300nA |
| 5.8 | 2.81mA | * | 4.3 | 56.2uA | * | 3.91 | 200nA |
| 5.7 | 2.62mA | * | 4.25 | 35.5uA | * | 3.9 | 125nA |
| 5.6 | 2.42mA | * | 4.2 | 22.0uA | * | 3.86 | 15nA |
| | | * | | | * | 3.85 | 2.5nA |

## Interpretation of ONS and Failure Analysis

**Background.** The ONS signature was originally discovered in early 1993 while performing CIVA (Charge Induced Voltage Alteration)[6] on some CMOS EPROM Icc failures with suspected floating nodes. CIVA uses a constant current source to bias a part while subjecting it to an electron beam in a Scanning Electron Microscope (SEM) for the purpose of direct identification of floating nodes. The parts yielded nothing but chaotic impulse noise rendering CIVA ineffective in these cases. Subsequent Failure Analysis revealed the cause of failure was due to a ruptured gate oxide in the array decoder. Since that time, a number of failures have been quickly prescreened as suspected gate oxide failures and subsequently proven as gate oxide failures with conventional analytical methods such as Emission Microscopy and Passive Voltage Contrast.

**Case Histories (Gate Oxide ONS).** The following waveforms in photos 1-7 were obtained by connecting J2 to an analog oscilloscope (AC input) and capturing the waveform real-time directly from the screen with the digital camera of the Alpha Innotech IS-1000 Emission Microscope and a 12.5 mm camera lens (Frame capture = 1/30 second).

The gain set-point of R7 is set to maximum (ONS sensitivity).

The Vcc across the DUT (Compliance voltage) is set at 5 volts using potentiometer R6 on a reference part measured through connector J2 on a voltmeter.

All parts tested in this section are 1 Megabit CMOS EPROM's incorporating 1.2 um, single metal, double poly technology.

*Photo 1* is an ONS signature from a functional row decoder failure which passes the production Icc standby test limit (100 uA). Icc standby can be determined with the ONS circuit by using the lookup table (table 1), 4.29 volts is approximately 50 uA. Note that the measured Icc is below the specification limit, however, the noise signature is present. In this case it is due to "wounded" gate oxide associated with the row decoder as determined by subsequent failure analysis.

Note: The ONS LED was observed to flicker intermittently, analogous to an aged neon lamp.

*Photo 2* is the absence of the ONS signature from a reference part. The ONS LED was inactive with the reference part. Icc = 30 uA (4.24 volts from the table).

*Photo 3* is a moderate to low level noise signature on part #2. This device fails to program. Icc = 30 uA (4.24 volts from the table). Note that the measured Icc is similar to the reference part, however, the noise signature is present. In this case the part failed due to "wounded" gate oxide associated with the row block decoder (a group of 4 rows was affected) as determined by subsequent failure analysis.

The ONS LED was observed to flicker intermittently.

*Photo 4* is a low level noise signature on part #3. This device has a failing row block decoder. Icc = 30 uA (4.24 volts from the table). Note that the measured Icc is similar to the reference part, however, the noise signature is present. This part also failed due to "wounded" gate oxide associated with the row block decoder as determined by subsequent failure analysis.

The ONS LED was observed to flicker intermittently once every 0.1 to 0.5 seconds.

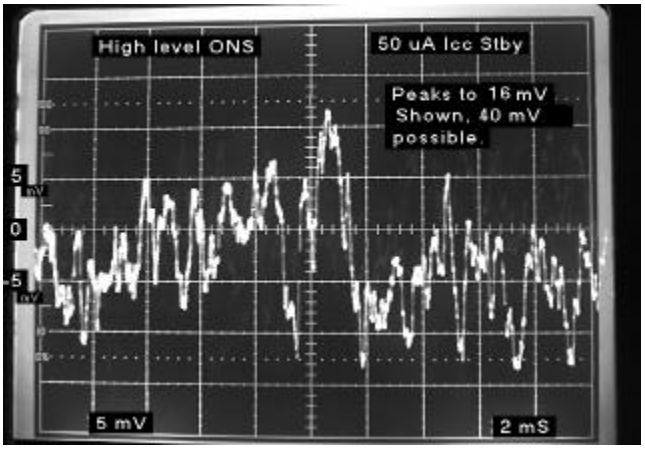



**Photo 1 Impulse noise (ONS) from Part #1, a CMOS 1 Meg EPROM in Icc standby. Noise peaks as high as 40 mV were observed over a period of 10 seconds.**

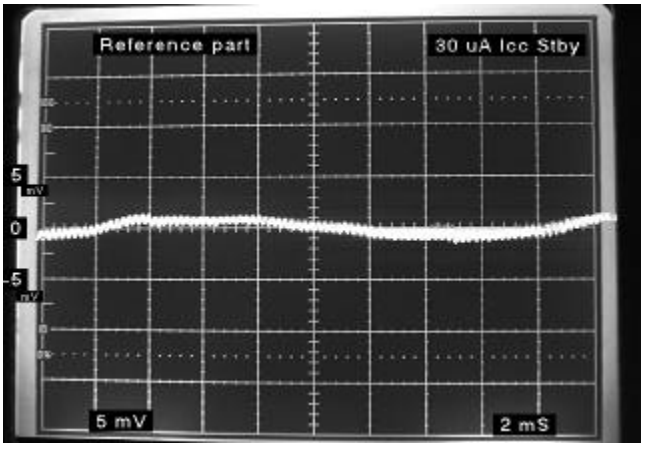



**Photo 2 Absence of the ONS signature from a reference part in standby.**

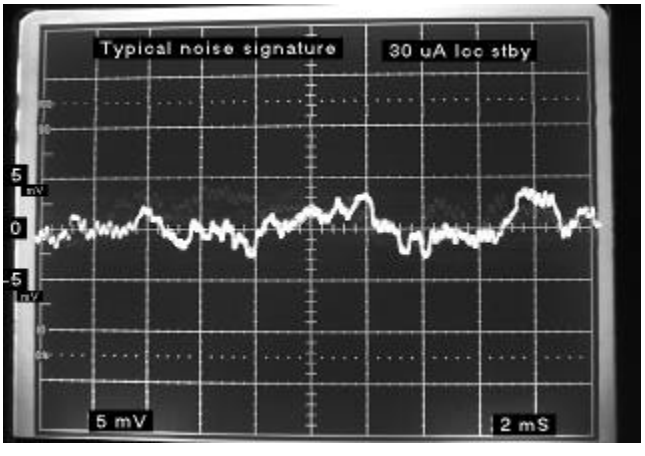



**Photo 3 Impulse noise (ONS) from a CMOS 1 Meg EPROM in standby. Part #2**

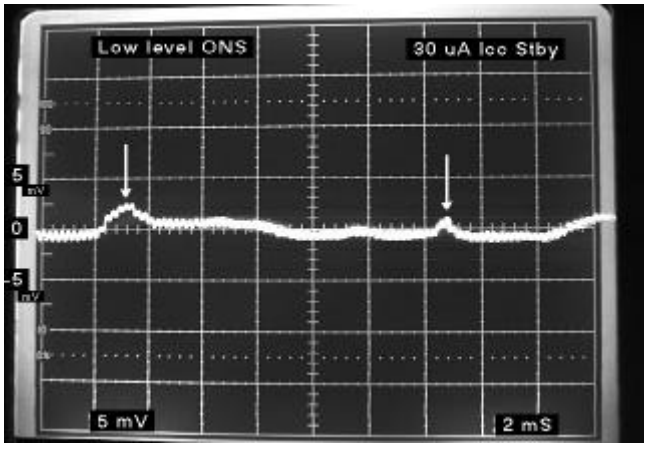



**Photo 4 Low level impulse noise (ONS) on part #3.**

*Photo 5* is a noise signature associated with part #4 which has a higher level of Icc: 4.75 mA (6.8 volts from the table). The ONS LED was observed to flicker intermittently.
Notice there is no correlation between the magnitude of Icc and the magnitude of the ONS signal. Gate oxides which have been overstressed to the point of a resistive short generate little to no ONS signal. Conventional test methods normally screen these types of Icc failures. The failure was subsequently isolated with emission microscopy to a ruptured gate in the row block decoder.

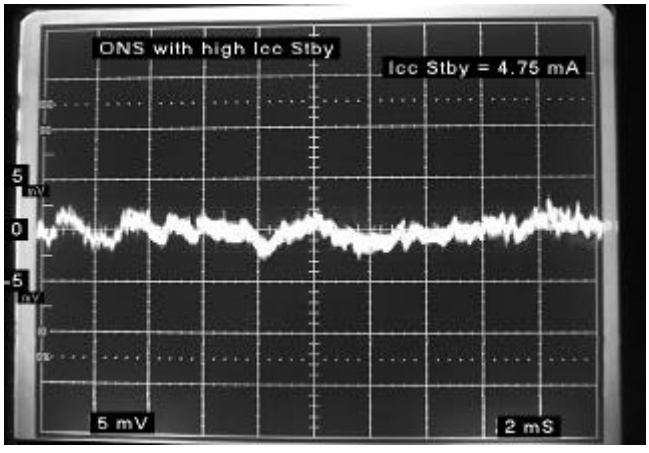



**Photo 5 Impulse noise (ONS) on part #4 which has a higher level of Icc. Note the signal level is reduced due to the resistive nature of the overstressed gate oxide.**

*Photo 6* is what is expected on a reference part with 2 feet of wire connected to an unshielded switchbox. The ONS LED is illuminated at a continuous moderate intensity. Remember the LED must flicker randomly or there is no noise signature.

*Photo 7* is an ONS signal superimposed on the stray AC signal for part #2 with 2 feet of wire connected to an unshielded switchbox. The ONS LED was observed to flicker randomly from a moderate to bright intensity.

Note that the oscilloscope is unnecessary for normal ONS testing. Only the ONS LED is required to show ONS, however, these examples were provided to show correlation between the oscilloscope and the ONS indicator.

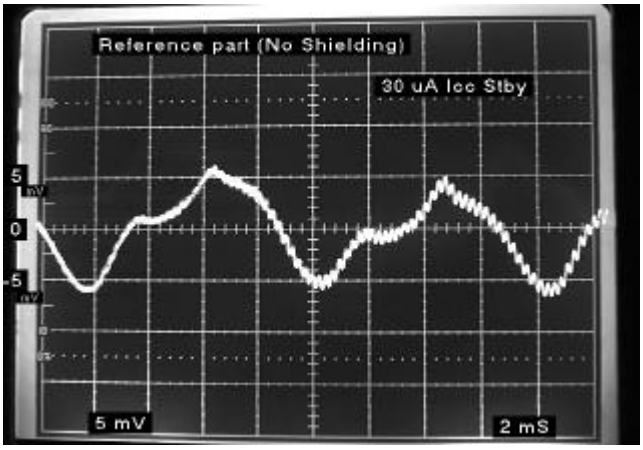



**Photo 6 Waveform from a stray AC signal on a reference part with 2 feet of wire connected to an unshielded switchbox.**

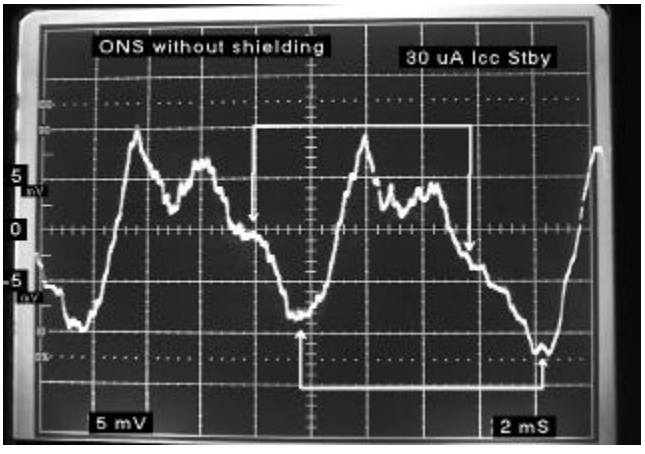



**Photo 7 is an ONS signal superimposed on the stray AC signal for part #2.**

**Emission Microscopy and Passive Voltage Contrast**. Once a part has been identified with an ONS signature, two phenomena become immediately evident:
1. The failure must emit light from the ONS defect.
2. The device has an established instability.

Since the constant current source is biasing a spark gap, photons will be generated. The detection success of the generated photons will depend on the overlying geometry. Note that liquid crystal is avoided in these cases due to the risk of overstressing the defect with sustained high current during analysis.

A 256K EPROM was identified to have an oxide noise signature. Emission Microscopy was used to identify any potential emission sites on the die. A site was identified associated with an EPROM row as shown in photo 8.

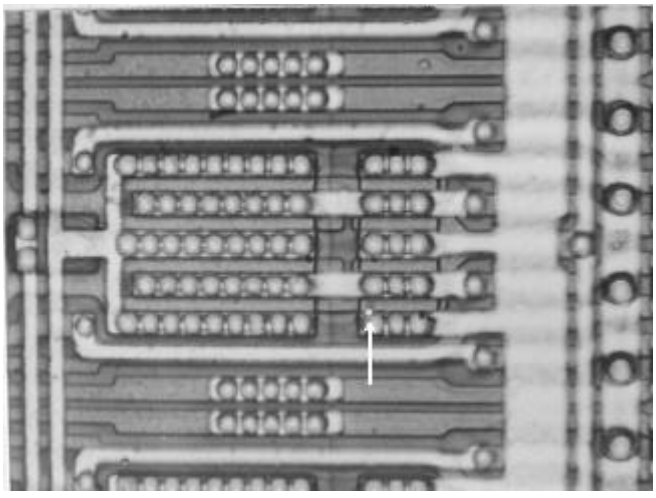


**Photo 8 Emission image associated with an EPROM row.**

The shape and location of the emission area indicates compromised gate oxide. Passive Voltage Contrast can be performed next by deprocessing the product to expose the poly and placing the properly grounded part in the SEM. A tilt angle of $60^0$ and a beam energy of 2 KV is all that is required to perform PVC. The electron beam charges the floating gate oxides positively due to the tilt angle allowing any compromised oxides to be quickly identified. Refer to Photo 9.

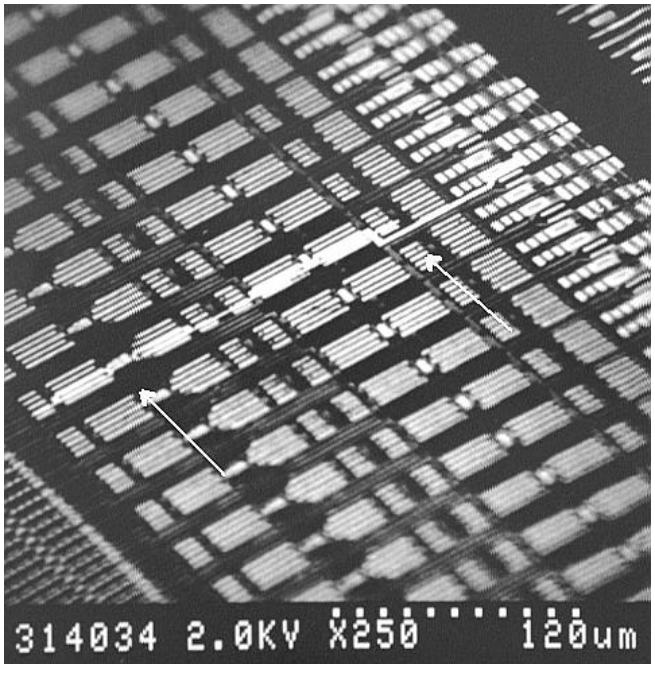



**Photo 9 Passive Voltage Contrast image of the failing gate structure.**

The poly layer was removed and the gate oxide defect imaged in the SEM. Refer to Photo 10. PVC was optional in this case due to the emission results, however, had emission been inconclusive, PVC could be used to quickly survey the die at the poly level for the gate failure.

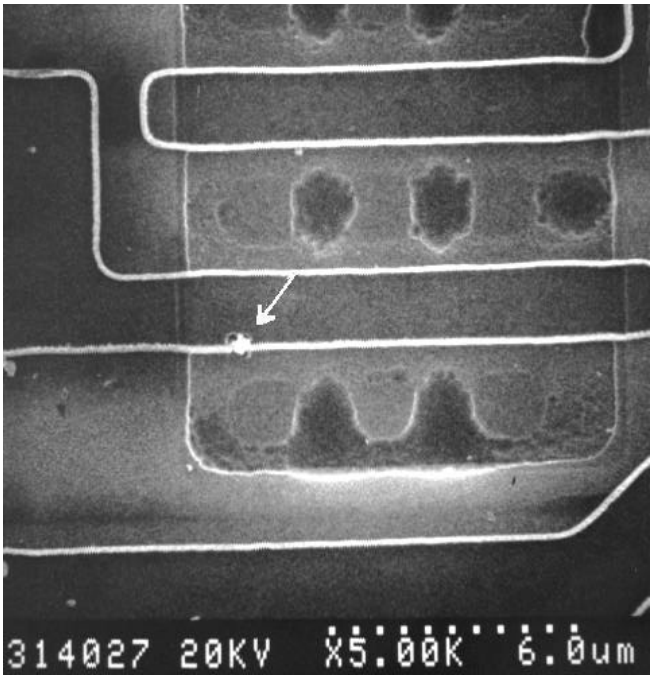



**Photo 10 SEM image of the oxide integrity defect after removal of the poly layer.**

**Yield Analysis of Metal/Oxide/Metal Interface Failures**

Metal particles between or across established metal lines which are not short circuits can have an extremely thin oxide interface as the only electrical isolation. These parts will eventually fail with stress. A .8 um double metal, double poly, EPROM process was analyzed at the yield analysis level for Icc and functional fallout. 20 representative failures from a group of wafers which were sorted and inked were assembled into packages for analysis. Three of the 20 assembled units tested had an ONS signature.
An analysis typical of this type of failure follows:
The ONS signature was observed to be extremely unstable with Vcc fluctuations as high as ± 0.5 volts on a part in Icc standby. The standby current at 5 volts was 150 uA. Due to the presence of ONS, photons will be generated from the spark gap with a visible spectrum. The part was biased and emission microscopy used to identify any potential emission sites on the die. A site was identified (using a 30 second integration time) associated with the EPROM y-decode area as shown in Photos 11,12, and 13. Photo 14 is an SEM image of the metal particle responsible for the metal to metal short as identified by ONS and Emission Microscopy. Notice the location of the spark gap indicated by the arrow.

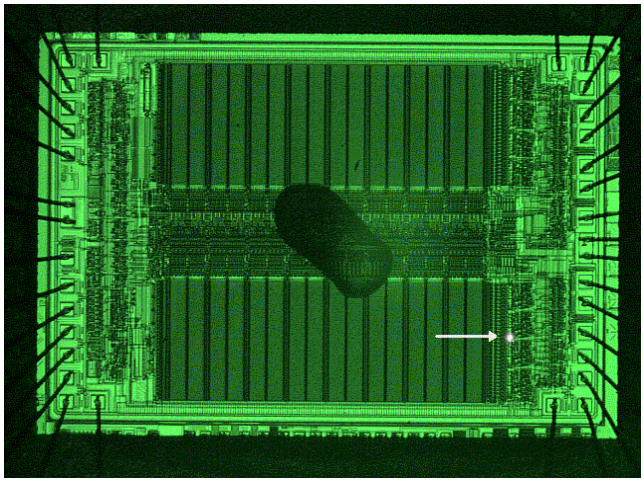


**Photo 11 Emission image in the EPROM y-decoder area.**

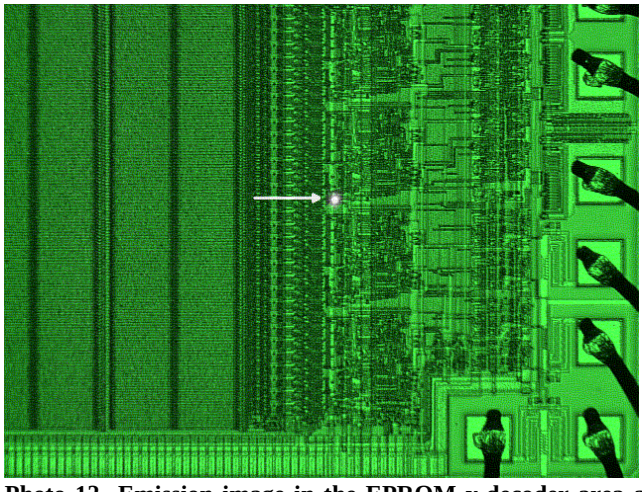


**Photo 12 Emission image in the EPROM y-decoder area at increased magnification.**

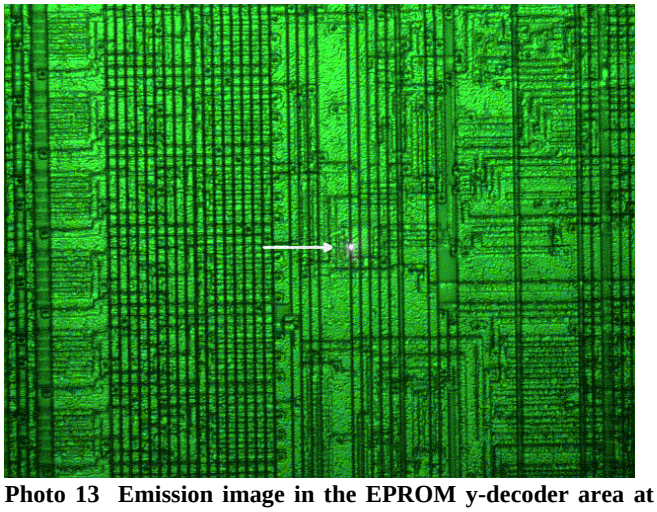


**Photo 13 Emission image in the EPROM y-decoder area at increased magnification.**

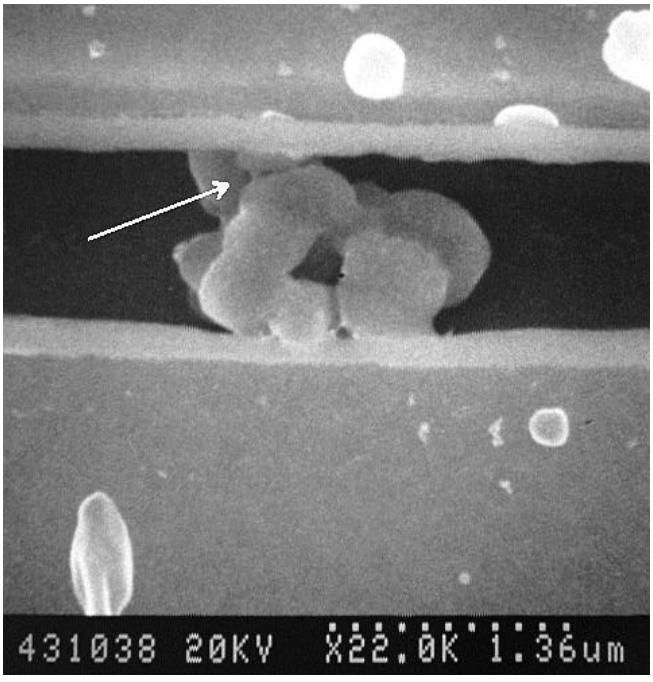



**Photo 14 SEM image of the metal particle responsible for the metal to metal short as identified by ONS and Emission Microscopy. Notice the location of the spark gap indicated by the arrow.**

## Wafer Level Reliability Testing

Performing the ONS test at the wafer level will require isolation of the decoupling capacitors which are typically associated with the probe card and or probe ring on the tester. An appropriate microminiature relay can be used in series with the decoupling path to Vcc, however, lead lengths must be kept to a minimum to ensure proper decoupling when the relay is active. The ONS circuit typically requires a 1 second settle time before measure. If this delay is unacceptable, R2 may be safely reduced to 50KΩ in order to decrease the settle time to 0.5 seconds.
The ONS detector circuit will need to be modified as shown below to create an output compatible with test:

1. Remove R8 and the ONS indicator.
2. Change the +12 supply on U4 to +5.
3. Install the diode, resistor, and capacitor as shown in figure 3.

The 22uF capacitor serves as an integrator to help latch the ONS data high for measurement by the tester. The Voh should be set at 3 volts for the tester to confirm a positive reading. When testing for ONS, remember that the outputs need to be tristated or in a no load condition (IDDQ test conditions), and ensure proper shielding is incorporated.

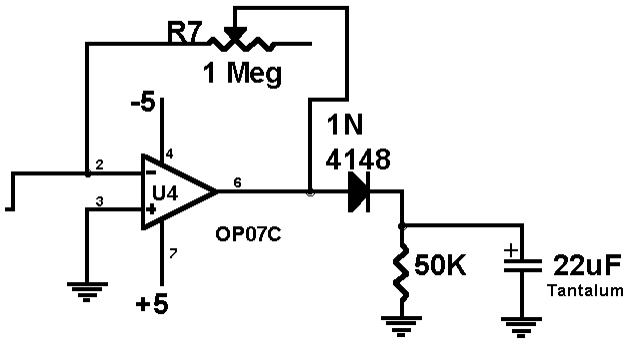



**Figure 3** Modifications necessary to the detector from figure 1 for the production tester interface.

## Package Level Testing

The same modifications apply to package level test as shown in Figure 3 and described in the WLR testing section. Remember that if decoupling exists on the DUT loadboard, ONS will be totally masked from detection as described in the previous section. The author strongly recommends the identification of several control unit failures with ONS identified through yield or failure analysis in order to "fine tune" the final ONS test system. Adding the ONS test bin will allow the reliability issue of weak oxides to be identified. The same disposition rules that apply to FAB lots with low yield should also apply to ONS therefore, it is recommended that "good units" from an identified lot with significant fallout for ONS be scrapped due to the obvious reliability implications.

## Failure Mechanisms

ONS detects thin oxide interface failures under bias through Icc or a discrete pin leakage. Some of the potential defects which can generate ONS follow: LESD (Gate oxide level), gate oxide integrity (Icc standby failures), metal/oxide/metal interface failures (Metal step coverage, metal particles, and dendrites) and metal/oxide/poly interface failures.

## Alternative ONS Detection Methods

If the laboratory is equipped with OBIC (Optical Beam Induced Current) measurement techniques, or CIVA[7] (Charge Induced Voltage Alteration) ONS can be detected; in the case of OBIC, by simply biasing the device with the OBIC source and measuring the change in current values as monitored on the screen. Since OBIC is designed to measure minute changes in current through a current amplifier, the image shows noise if ONS is present.

In the case of CIVA, the existing constant current source is used to bias the pin leakage. The resulting CIVA signal will consist of band limited noise (if ONS is present) and can be directly imaged on the SEM slow scan screen.

## Conclusions

A new method to identify the presence of oxide integrity issues on a CMOS process has been presented. The Oxide Noise Signature method can identify compromised oxide interfaces associated with both functionally failing devices and "good" devices[8] while biased in an Icc standby mode or associated with a pin leakage. The leakage or Icc standby values can be at or below specification and still be identified as a failure with ONS, whereas IDDQ testing measures only Icc values, ONS checks the stability of the Icc to the device. Products can be statistically sampled, without in-depth analysis, to identify these instabilities. Case histories of mechanisms which generate ONS have been presented with emphasis on gate oxide and metal/oxide/metal failure mechanisms. The ONS signal has been shown to be an indicator that visible photon emission is occurring from the defect (spark gap) and is identifiable with tools such as Emission Microscopy and Passive Voltage Contrast.

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