

Stress Reduction during Silicon Thinning Using Thermal Relaxation and 3D Curvature Correction Techniques

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Abstract

Backside sample preparation is required by many post silicon validation techniques like FIB (Focused Ion Beam) circuit editing and optical probing using Photon Emission or Laser Stimulus methods [1]. In spite of many conventional methods of silicon thinning and polishing, some challenges remain as new packages are introduced. With large die packages the issue of cracking during backside thinning is arising due to package curvature stress. 3D profile methods will be shown in conjunction with thermal relaxation to alleviate silicon center to edge variance allowing sample prep of large areas with thicknesses below 10 μ m. Thinning and polishing methods will be shown to be interactive with the device heated; demonstrating both thermal stress reduction coupled with curvature reduction.

Introduction

Warpage of the die is both well-known and commonplace in larger flip chip packages, as well as in stacked-die packages. Warpage is often designed into the component, so that at typical operational temperatures the package will 'relax', thus flattening the die and, in turn, producing a more effective interface with the package's heat-sink (metallic lid). For the failure analyst, the first step in previous backside sample preparation protocols has been for the lid to be mechanically removed -- meaning that the part's thermal profile is never taken into account. The method described here, with the obvious absence of the heat-sink, serves to replicate what happens to a part thermally in usage, thus taking advantage of known thermal design protocols.

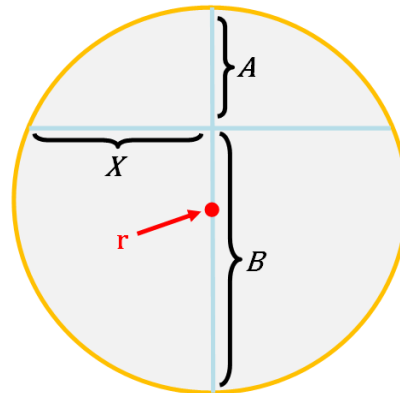
Although previous mounting efforts have helped redirect die stress yielding a part that allows for thinning with reduced crack risk [3], the issue of planarity and warpage of the die still arises. It has been discussed in previous papers that temperature cycling can help to reduce warpage of a die by 5-10 μ m, however, the core issue of internal stress has largely been ignored [2].

This paper, for the first time, explores use of thermal relaxation to reduce stress during silicon thinning and

polishing, yielding improved planarity across large dies. To test the effects of thermal relaxation on a part during and after thinning, BGAs with 400mm² (20x20mm) dies were used. All parts were thinned and polished on the Ultra Tec Manufacturing's ASAP-1 IPS Digital preparation tool with a maintained temperature through the entire thinning/polishing process. Modeling data will show a basic exponential relationship of the silicon surface contour. The issue of changing stress and curvature during thinning and strategies to mitigate variant thermal expansion of the tool and device will be discussed.

Background

Normally lens curvature calculations are measured in Diopters. Diopter calculation can be done first by calculating radius and then converting it into Diopters using the index 1.523 for crown glass. Equations 1 & 2 show how radius of curvature was calculated. Diopter conversion is shown in Equation 3.



$$X^2 = A * B \quad [\text{Eq. 1}]$$

$$r = \frac{(A + B)}{2} \quad [\text{Eq. 2}]$$

$$D = \frac{523}{r}; \quad [\text{Eq. 3}]$$

Index 1.523 for Crown Glass
Units: Diopters

This convenient model, however, is not ideal as it is designed for spherical curvature calculations. Therefore a BGA device with a 400mm² die was used to measure the z variance at 10 points from center to edge. The die is symmetrically curved from the center so any radius vector may be chosen as long as the x-y plane of the device is perpendicular to z. The resulting curve is shown in Figure 1.

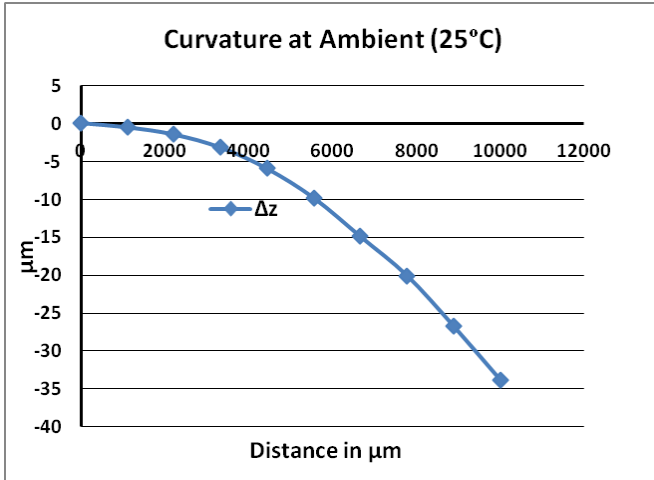


Figure 1: Graph showing normal curvature of an unthinned part at ambient.

As the diopter calculation is mainly for lenses, the data used in Figure 1 was used to generate a regression equation [7] as shown below:

$$\Delta z = -3.4 E^{-7} r^2 + 0.00085r + 0.11;$$

r = radius distance from origin,

Δz = delta z curvature from 0, 0, 0 (origin).

Since the latter part of the equation has relatively small values, they can be disregarded leaving us with:

$$\Delta z = -3.4E^{-7}r^2 \text{ [Eq. 4]}$$

Equation 4 above now represents a more accurate representation of the curvature as it takes into account multiple regression points rather than assuming 3 points on a sphere. Later, it will be shown only 2 points are actually needed to model accurately the surface.

Thinning without Thermal Relaxation

A BGA with initial die thickness of $\sim 700\mu\text{m}$ was first mounted and prepared under normal conditions. The part initially was thinned down to $500\mu\text{m}$ on the ASAP-1 sample preparation system. The inspection of the sample after only $200\mu\text{m}$ silicon removal showed that the die cracked at many points. Further investigation on additional units revealed cracking at the beginning of the thinning process due to high curvature stress.

To minimize the crack risk, another part was mounted and thinned at 25°C (ambient temperature) on the ASAP-1 IPS now with a controlled force feedback fast stepped at 40nm which allowed for a finer removal process. The initial curvature of the die was $\sim 40\mu\text{m}$ before thinning. The part was inspected after $100\mu\text{m}$ of silicon removal and showed no sign of cracking. After further thinning and polishing down to $120\mu\text{m}$, the center to edge height variation was measured to be $\sim 64\mu\text{m}$. The package curvature was observed to actually increase with thinning as the die contributed less counterforce to the package.

Figure 2 below shows the silicon fringe pattern of the part prepared at ambient temperature. Fringes that are closer together show the increasing warpage.

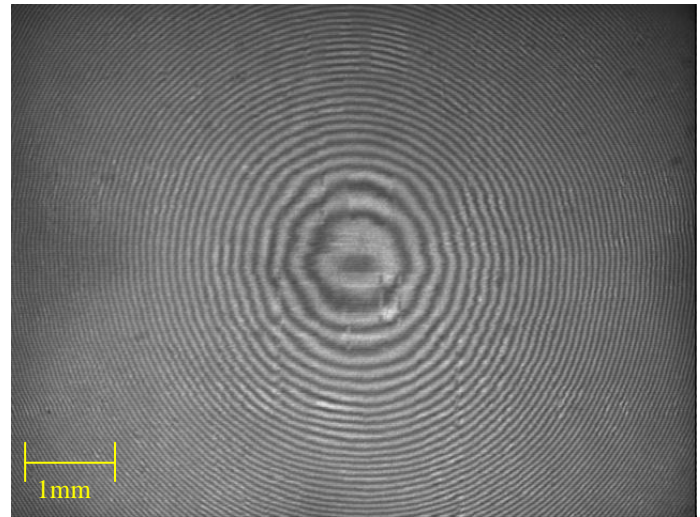


Figure 2: Fringe pattern of part prepared at ambient temperature.

Note: The number of fringes when measured is temperature independent.

Figure 3 was generated by counting fringes from center to edge of the die in increments that allowed for 10 data points. Refer to fringe counts conversion to silicon depth in Equation 7 and 8 shown later in the paper.

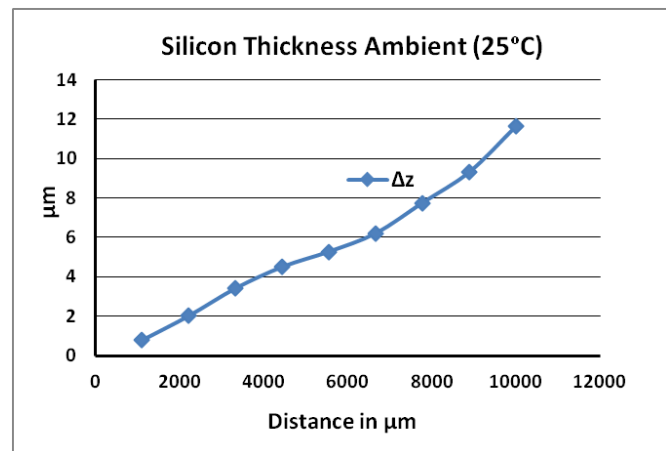


Figure 3: Graph showing change in silicon thickness locally after thinning and polishing the part at ambient temperature.

The regression equation generated for the silicon thickness of a part prepared at 25°C is:

$$\Delta z = 3.8 E^{-8} r^2 + 0.00073r + 0.13; \text{ [Eq. 5]}$$

$$\Delta z = 3.8 E^{-8} r^2 \text{ [Eq. 6]}$$

Thermal Relaxation and Thinning

To see the effect of thermal relaxation on the die, the die thickness center to edge without heating and then with the part heated at 80°C and 110°C are compared in Table 1. The measurements show that elevating the temperature of the part significantly reduced the warpage. For simplicity, a Diopter meter was used for comparison of the die curvature reduction with temperature.

Temperature	25°C	80°C	110°C
Δz^* (μm)	39.15	11.73	1.24
r (mm)	1152.64	3848.62	36391.13
Diopters (for n =1.523)	0.45	0.14	0.01
*x travel = 9.5mm from center			

Table 1: Thickness Variation with Temperature.

Figure 4 shows graphically the decreasing warpage and radius of curvature of the silicon as temperature is elevated. This is expected since the under fill is typically cured around 110°C. The different coefficients of expansion are more closely matched relaxing the stress on the die thus minimizing cracking risk.

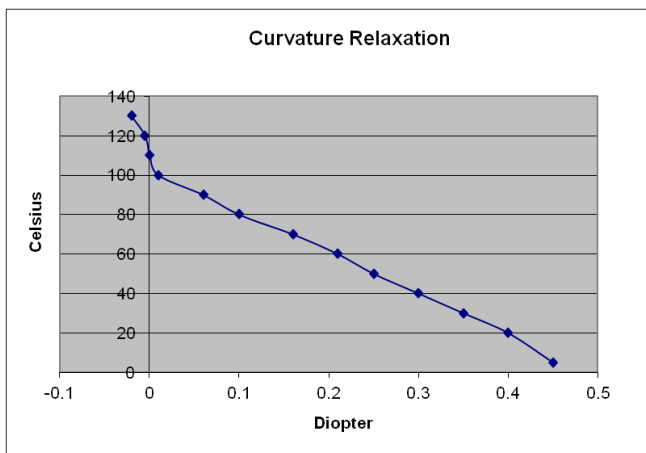


Figure 4: Graph showing warpage reduction as temperature is elevated.

To decrease the original 64 μm of center to edge height variation, another sample part was mounted on the ASAP IPS thermal fixture with 4 nylon screws to minimize stress on the part and heated at 80°C (Figure 5 & 6). After thinning 100 μm at 80°C, the part showed no sign of cracking proving that thermally isolating the sample can indeed relax the part. By relaxing the stress thermally, the silicon can be removed more aggressively. However,

the next step was to see how planar the sample was after thinning and polishing down to 120 μm of remaining silicon. The 80°C thinned and polished part was measured for planarity using an IR microscope and the fringe counting method shown in Ref 1. The paper explains how counting the fringes on the interference pattern seen under an IR microscope can be converted into silicon depth in μm . Equation 8 was used to calculate the thickness variance on the parts thinned at various temperatures.

$$\Delta t = \frac{(\lambda * OPD)}{2 * n}; \text{ [Eq. 7]}$$

n = index of refraction = 3.434 for silicon
 Δt = change in silicon thickness.
 λ = wavelength of light = 1.064 μm
 OPD = number of observed fringes. [1]

Putting the constants (n and λ) into the equation is simplified as Equation 8 below:

$$\Delta t = OPD * 0.155 \text{ [Eq. 8]}$$

Temperature	25°C	80°C	110°C
Fringe Count*	415	177	75
μm Conversation	64	27	12
r (mm)	781.28	1851.87	4166.67
Diopters (for n =1.523)	0.66	0.28	0.13
* x travel = 10mm from center			

Table 2: Table showing fringe count of polished silicon, μm conversion and Diopter Conversion

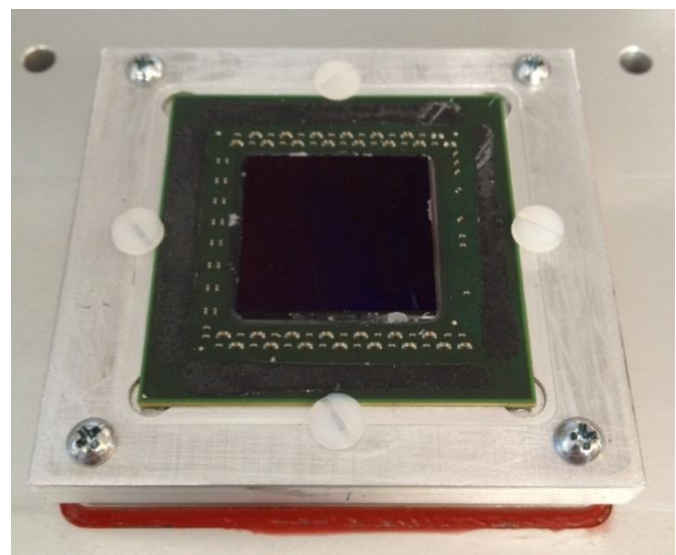


Figure 5: BGA mounted with Nylon Screws on the ASAP-1 IPS Thermal Plate

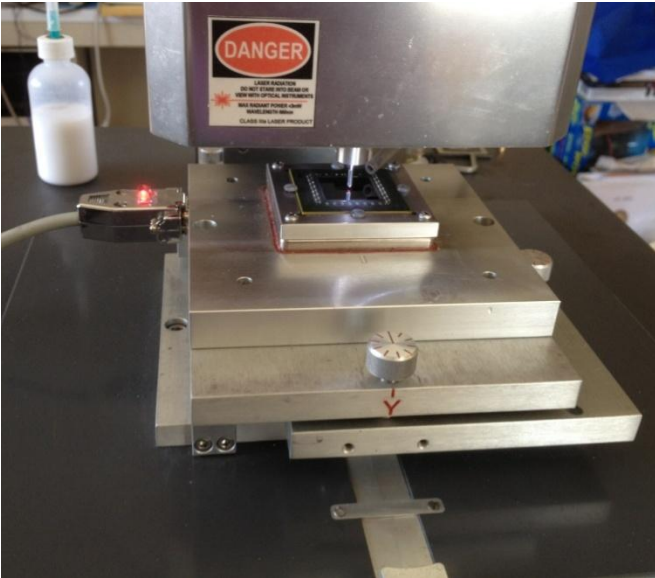


Figure 6: Thermal mounting set up on ASAP-1 IPS

The interference fringe pattern for the part prepared at 80°C is shown in Figures 7 and 8. The fringe count for the 80°C part was 177 therefore the change in silicon thickness from center to edge was $\sim 27.43\mu\text{m}$. This deviation can be explained as the warpage of the package is taken into account once the part is back to ambient temperature. To confirm this, the part was then mounted die side down and measured for variance from center to edge at ambient temperature and then heated up to 80°C. As shown in Table 3, the package variance at 80°C was $\sim 24.84\mu\text{m}$ which is very close to $27\mu\text{m}$ showing that the package contributes to the warpage even with thinned Si.

Temperature	25°C	80°C	110°C
Δz^* (μm)	47.64	24.84	12
r (mm)	1049.56	1851.87	4166.67
Diopters for n =1.523	-0.49	-0.28	-0.13
* x travel = 10mm from center			

Table 3: Curvature reading showing bending of the package itself.

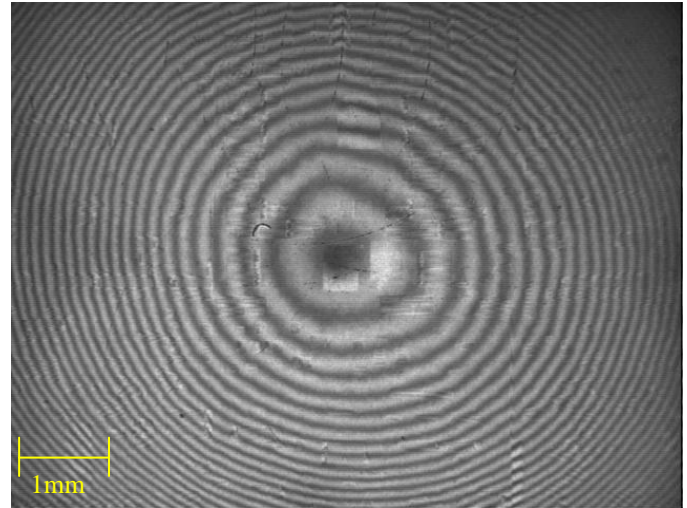


Figure 7: Fringe pattern of 80°C prepared part

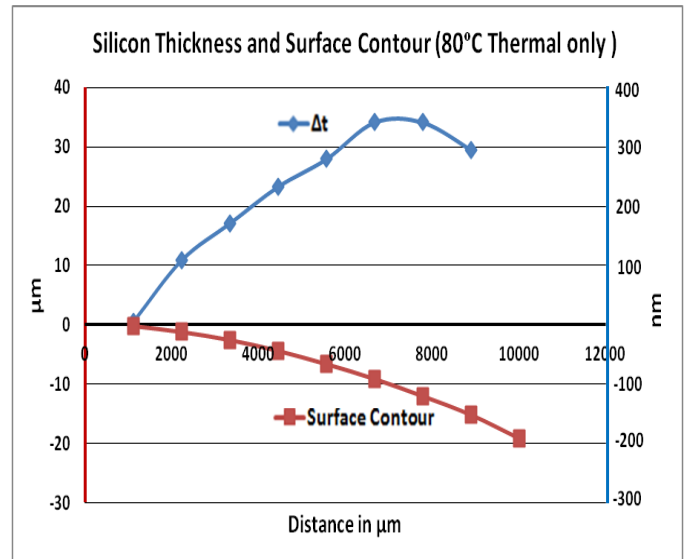


Figure 8: Graph showing silicon thickness vs. surface contour center to edge on a part prepared at 80°C.

The regression equation generated for the silicon thickness of a part prepared at 80°C is:

$$\Delta z = -4.3 E^{-8} r^2 + 0.00078r \pm 0.24 ; [\text{Eq. 9}]$$

$$\Delta z = -4.3 E^{-8} r^2 [\text{Eq. 10}]$$

The regression equation generated for the surface contour of a part prepared at 80°C is:

$$\Delta z = -1.6 e^{-7} x^2 + -0.0029x + 0.16; [\text{Eq. 11}]$$

$$\Delta z = -1.6 E^{-7} r^2 [\text{Eq. 12}]$$

To further illustrate that thinning and polishing at a higher temperature can yield a flatter sample, a part was prepared at 110°C and the Fringe pattern is shown below in Figure 9.

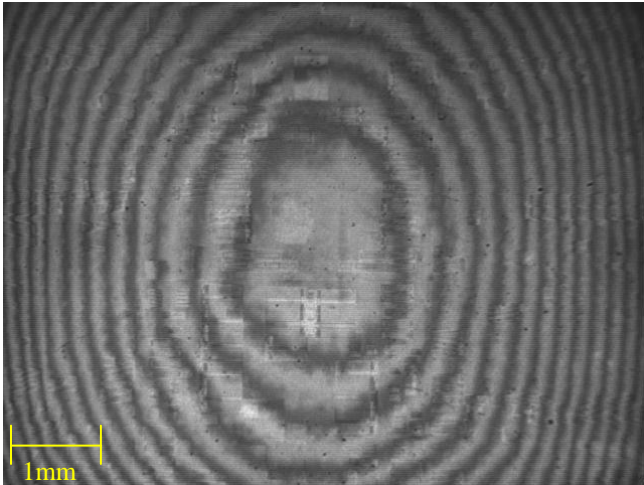


Figure 9: Fringe pattern of 110°C prepared part

Comparing the fringe counts as shown in Table 2, fewer fringe counts were measured on a 80°C and 110°C prepared part than the part prepared at ambient temperature. A 110°C part had 102 less fringe counts than at 80°C part therefore curvature change is less, showing that flatter samples can be achieved with higher temperature.

Figure 10 shows a visual comparison of the curvature relaxation showing how the pattern of venetian blinds reflected off surface at 25°C (image on top) becoming parallel and therefore flat at 110°C (image on bottom). The wave-front error is demonstratively quite low as evidenced by the image quality of the reflected image.

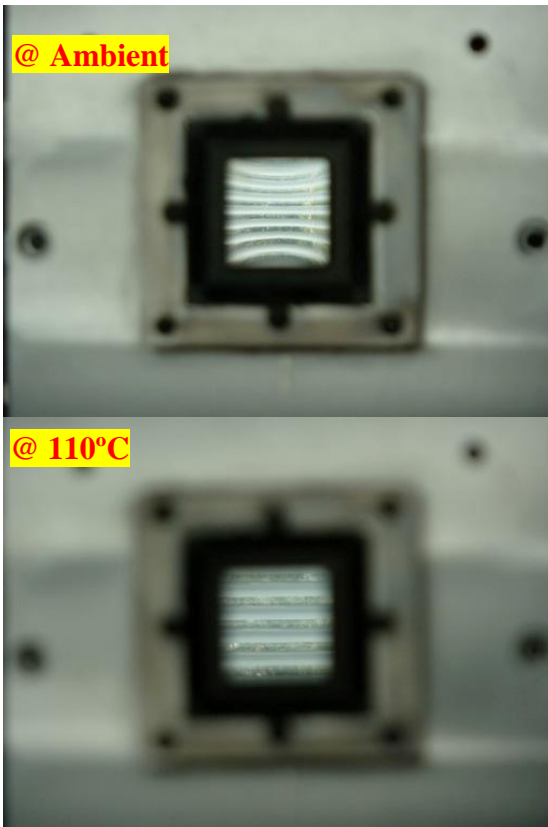


Figure 10: Visible interpretation of curvature relaxation.

By introducing a thermally controlled environment to the device during the thinning and polishing process, the warpage and stress of the die is significantly reduced and therefore yields a more planar surface as well as a better polish.

Thinning with Thermal and 3D Curvature Technique

Since thermal relaxation alone may not account for the remaining curvature on the die, an exponential 3D curvature correction technique was used. It is calculated by taking several Z depth measurements. The difference between the edges to center is then converted to the form:

$$z = A x^2; \text{ [Eq. 13]}$$

where A is the calculated constant fitting the data.

The ASAP-1 IPS uses Equation 13 to contour the sample while thinning. Z height is calculated as a function of radius position from the centroid.

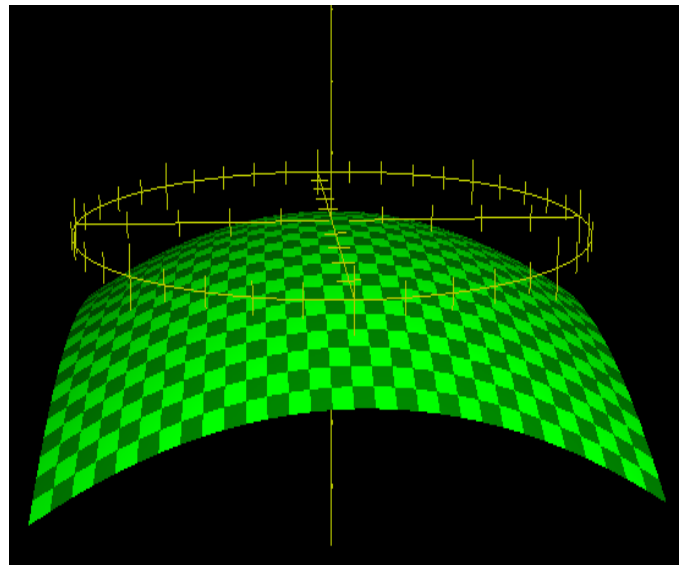


Figure 11: Contour model of die surface curvature.

Figure 11 shows the contour model of a die surface curvature. With the improved x^2 representation of the equation, any number of squares on the structure can be locally polished with the active contour allowing pockets in separate areas to be defined or the whole area to be opened. The new regression fit requires just the center and 1 radius data point since the part is tilt corrected. The 3rd point is assumed to be mirror symmetric on the axis. Although the paper emphasizes this model based on typical under-fill products, other custom known stress curves can be used.

To test this, a new part was mounted on the thermal plate of the ASAP-1 IPS and was heated to 80°C. The 3D curvature technique was used to thin and polish another 400mm² BGA sample. An initial radius of curvature

reading of the part at 25°C was 1387.2mm and ~35µm center to edge z height variance. After heating it at 80°C the curvature was measured to be at 4999.9mm and ~ 11µm center to edge z height variance. Looking at the resulting fringe patterns shown in Figures 12 and 13 and comparing them to the fringe patterns of an 80°C prepared part as shown in Figure 7, it is visible that thermal relaxation with 3D correction yielded a much flatter surface after contouring the curvature. This is evidenced by the fringes being spread out over the die.

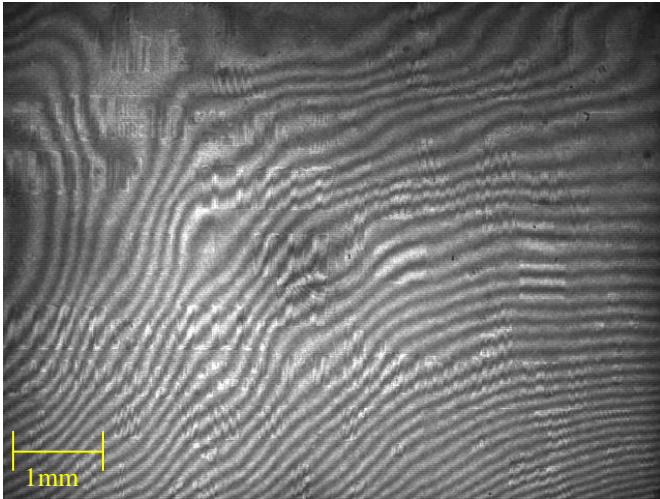


Figure 12: Fringe pattern at center of an 80°C prepared part with 3D curvature correction.

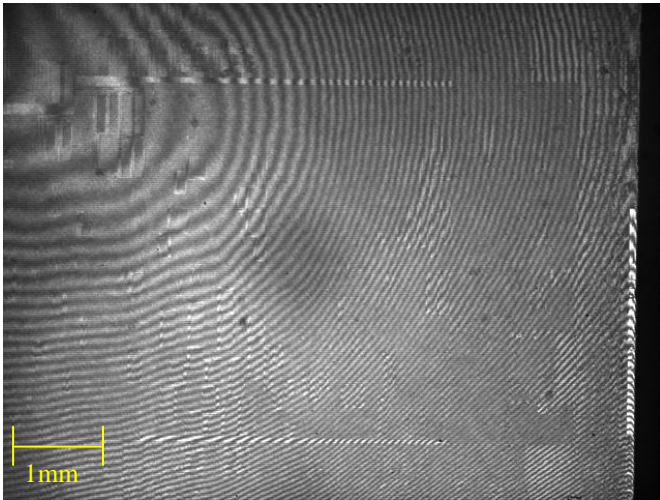


Figure 13: Fringe pattern at edge of an 80°C prepared part with 3D curvature correction. Package relaxation during thinning contributes curve error and once known can be compensated for on future parts.

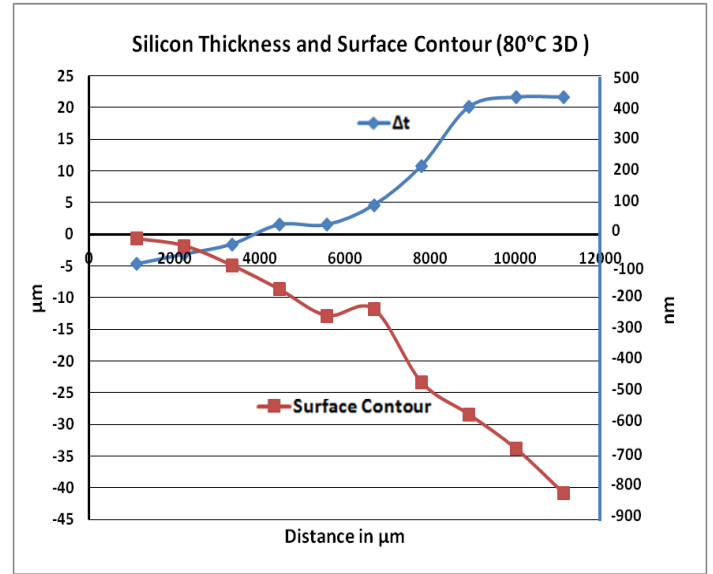


Figure 14: Graph showing silicon thickness and surface contour center to edge on a part prepared at 80°C and using 3D curvature correction.

The regression equation generated for the surface contour of a part prepared at 80°C + 3D:

$$\Delta z = -2 E^{-7} r^2 + -0.001r + 0.8; \text{ [Eq. 14]}$$

$$\Delta z = -2 E^{-7} r^2 \text{ [Eq. 15]}$$

Issues with Thermal Heating

With curvature thinning, it is known that the edges will be relatively flatter than the center due to the nature of the tools and their cylindrical shape if the tool is not stepped to the edge of the die. [5] It is important to note that this shape of the tool will cause errors in radius measurements. Additionally, expansion of the tools needs to be taken into consideration while using the Thermal Technique.

The equation of linear expansion is expressed as:

$$dl = L_0 \alpha (t_1 - t_0); \text{ [Eq. 16]}$$

dl = change in length (m, inches)

L₀ = initial length (m, inches)

α = linear expansion coefficient (m/m°C, in/in°F)

t₀ = initial temperature (°C, °F)

t₁ = final temperature (°C, °F) [6]

Tool Material	Linear Temperature Expansion Coefficient (10 ⁻⁶ m/mK)	Thermal Conductivity k - W/(m.K)
Brass	18.7	109
Aluminum	22.2	250
Iron	12	80
Xylem	4	0.1

Table 4: Expansion Coefficient vs. Thermal Conductivity of Various Tool Materials.

With Brass tools, tool expansion at 80°C was measured to be 17µm in the center whereas on the edges it measured to be 8µm. This error is due to air turbulence impacting the temperature of the spindle and tool attached to the collet. Standard ASAP-1 xylem tools were used to mitigate this issue and a low cfm fan used to draw heat away from the spindle assembly reducing the effect to under a micron of error.

Conclusions

The challenge with silicon thinning for warpage and planarity of large dies has been addressed. As described in the paper, die curvature is greatly reduced as the part is thermally relaxed. Crack risk has been shown to be greatly reduced allowing complex thinning and pocket milling operations resulting in greater sample yield. Using thermal relaxation for stress reduction greatly reduced warpage of the die, thus yielding planar samples. 3D curve correction using exponential equations allowed thinning of silicon well under 10µm. By using modeling data, a basic exponential relationship of the silicon surface contour was generated. This took into account the curvature during thinning and polishing the dies. Combining 3D curve correction with thermal relaxation allowed for the flattest samples opening the door for large area thinning within a few microns of the active area from the backside.

References

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