BGA and Advanced Package Wire to Wire Bonding for Backside Emission Microscopy

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Abstract

A new method of preparation will be shown which allows traditional fixturing such as test heads and probe stations to be utilized in a normal test mode. No inverted boards cabled to a tester are needed since the die remains in its original package and is polished and rebonded to a new package carrier with the polished side facing upward. A simple pin reassignment is all that is needed to correct the reverse wire sequence after wire to wire bonding or wire to frame bonding in the new package frame. The resulting orientation eliminates many of the problems of backside microscopy since the resulting package orientation is now frontside. The low profile as a result of this technique allows short working distance objectives such as immersion lenses to be used across the die surface. Test equipment can be used in conjunction with analytical tools such as the emission microscope or focused ion beam due to the upright orientation of the polished backside silicon. The relationship between silicon thickness and transmission for various wavelengths of light will be shown. This preparation technique is applicable to advanced packaging methods and has the potential to become part of future assembly processes.

Introduction

Traditional backside emission microscopy requires the integrated circuit to be polished from the backside and socketed in special fixturing for inspection with near infrared energies through the polished silicon surface. Sample preparation for backside analysis requires the sample to remain in the original package or wafer and be imaged through the bottom of the socket that makes electrical contact to the integrated circuit. Certain types of BGA and Chipscale packages cannot be prepared for backside imaging. Current backside preparation equipment is costly and does not produce a flat surface, resulting in a lens effect through the silicon. The height of the socket and corresponding circuit board inhibit imaging at high magnification or with high numeric aperture due to the recessed pocket created in this configuration. The preparation methods shown in this paper allow an optically flat surface 15 µm or greater to be routinely obtainable to an accuracy of ±8 microns with carbide sandpaper and ±4 microns with diamond lapping film. Current CNC-type backside prep tools have an accuracy no better than ±50 microns. Real time laser interferometry for surface flatness with polished samples will be shown and analytical methods discussed.

Imaging through polished silicon

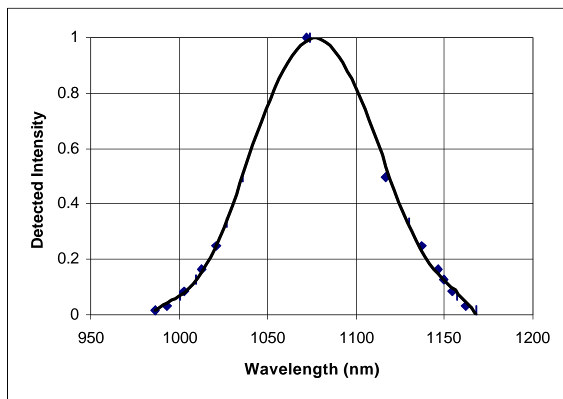
Currently, the methods for imaging with a CCD camera involve time integration to acquire enough light to form an image of the circuitry under examination. Real time infrared imaging from the polished backside of a silicon-based integrated circuit is difficult due to the low frame rates coupled with inadequate illumination intensity. Traditional methods of Near Infrared Imaging (NIR) use an optical filter in conjunction with a broad-spectrum illuminator such as a quartz halogen bulb. The desired wavelengths pass through the filter and are used in the microscope illuminating path. The desired wavelength of the source is selected by the filter rejecting the unwanted light. The filter will be degraded or destroyed due to heating if excessive intensity is used. As the filter bandwidth is narrowed, the total energy is also reduced from the output. Due to these constraints, the current illumination technology cannot provide bright, narrow bandwidth illumination.

Lasers are coherent by nature. A 1064nm continuous wave laser can be used as the illuminator source replacing the traditional filter and bulb approach. This illumination system differs from the laser scanning microscope in that the laser energy is injected into an ordinary fibercable attached to the emission microscope. Laser speckle is removed dynamically by an array of spinning multiple reflective surfaces. The bright source eliminates the need for integration allowing a quick determination of focal depth as well as navigation around the die. CCD cameras capable of rapid frame rates can function without the need for integration as well as minimizing the integration time required for frame rate CCD's. Real time navigation on a probe station or test head becomes the same as if the part were

viewed from the front side. Emission microscopy as well as backside sample preparation is simplified due to the ability to navigate and focus "real time" especially on thick or heavily doped samples.

The Silicon Filter Effect and Thinning

Backside imaging through the silicon results in filtration of the visible wavelengths and a portion of the NIR spectrum as shown in Graph 1. The data was generated by placing a dial monochromator between a CCD camera and an illuminated silicon filter 600 µm thick.[1] The resulting curve is a bandpass showing the detection limits of the CCD camera to the right and the attenuation of shorter wavelengths of light to the left. As the silicon is thinned, the bandpass widens allowing shorter wavelengths to pass.



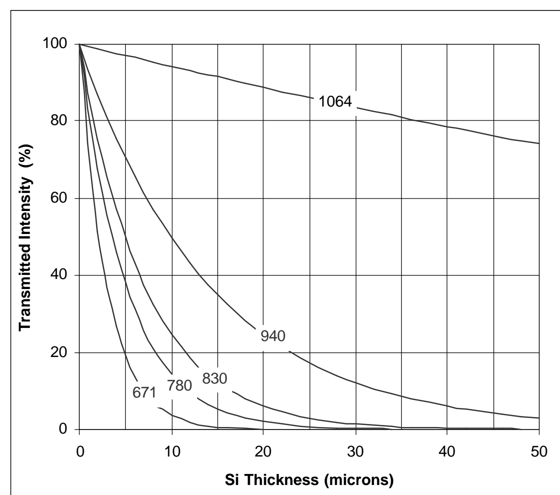
Graph 1. CCD camera to silicon bandpass curve through a 600 µm silicon filter.

The absorption curve is an exponential function as shown in Equation 1.[2] The total transmitted light through a solid of thickness t relies on the fractional attenuation of the light, independent of intensity, for a given wavelength. The absorption coefficient is selected based on a given wavelength of light.[3]

$$I(t) = I_0 e^{-\alpha t} \qquad (1)$$

I_0 = Incident Intensity
α = Absorption Coefficient
t = Thickness

Thinning the sample translates to increased emission sensitivity as well as improved optical resolution of the circuitry. The percent of transmitted light as a function of wavelength and thickness is shown in Graph 2 using five common laser lines. The selection of visible wavelengths of light allow endpointing of selectively etched windows in the backside of silicon using OBIC methods.[4] An ultimate target thickness to 5µm can be obtained, however, this technique requires active areas capable of producing an OBIC signal to be under the target area. OBIC endpointing can be used with all the polishing methods discussed in this paper if electrical connections are established in situ.



Graph 2. Transmission of light through silicon as a function of wavelength and thickness for λ = 671 nm, 780 nm, 830 nm, 940 nm, and 1064 nm respectively.

Focal Depth Measurement

The thickness of the remaining silicon shall be determined from Equation 2.[5]

$$\Delta F * n \cong t \qquad (2)$$

ΔF = Difference in focus from polished surface to circuit
n = Index of refraction of the silicon
t = thickness

Therefore the focal distance from the polished surface to the metallization multiplied by 3.434 = thickness of the remaining silicon at a wavelength of 1064 nm. This is the basis for determining tilt as well as thickness of the remaining silicon. Note: The Mitutoyo focus block on the microscope is graduated in microns. Calibrating for error is done with the chosen microscope objective (100X NIR) and a sample of known thickness. The index of refraction with the error factor combined is calculated for this focus mechanism by dividing the known thickness of a wafer by the focus distance from surface to circuit (249 µm/68 µm=3.66). Throughout this paper n=3.66 for silicon will be used pertaining to the focal measurement method. It is important to note the error in precision is compounded by the 3.66 multiplier, making precise focal point measurements tedious.

Sample Preparation

Preparation on an Ultra Tec Polisher

A 100 pin PQFP Cache RAM was selected for backside preparation. The integrated circuit that needs to be prepared for backside imaging is already packaged in a typical plastic epoxy package. If the package is of the open cavity (ceramic) or soft cavity type (such as with a diecoat), the cavity will need to be filled with a rigid material such as room temp cure epoxy prior to polishing or lapping the package material. Do not use a high temp epoxy! The stress of thermal contraction of the epoxy against the thinned die will distort and destroy it. In this case a standard molding compound is the encapsulant without die coat. Figure 1 is a photo of the 100 pin PQFP package mounted with hot melt wax on the center polishing plate of an Ultra Tec precision polishing jig. The die is placed roughly in the center and the plate labeled A, B, C, and D in conjunction with the two tilt control knobs. The tilt control knobs are shown in figure 2. Tilt control allows for compensation of the angle the die surface is lapped.

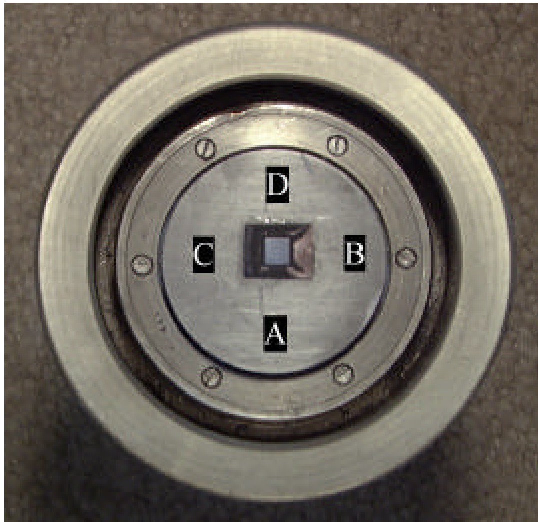


Figure 1. PQFP package attached to polishing jig. The markings A, B, C, and D will be used to planarize the die tilt.

Trigonometric Tilt Planarization

The bottom of the plastic package is mechanically lapped (sanded) or milled to expose the die attach paddle and the bottom of the die. Once the die is exposed, 1200 grit sandpaper is adhered to the main polishing wheel with water only. No PSA backing is needed. Polishing proceeds as shown in figure 3. The weights on the top of the jig supply 2000 grams of pressure on the sample in this instance. Only 2 minutes of polishing are required. The entire jig is placed inverted on the pedestal under the emission microscope optics as shown in figure 4.

Referring back to figure 1, the four corners of the die are imaged with the laser and the focal depth is measured from the surface of the silicon to the underlying circuitry. The corners are identified by the two adjacent labels to the respective corner. AB = 157 µm, BC = 161 µm, CD = 142 µm, and DA = 135 µm. The die circuitry is obviously not planar to the jig.

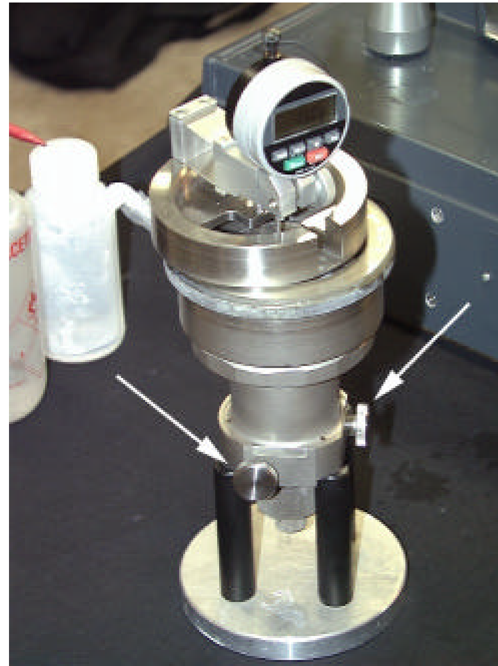


Figure 2. Precision polishing jig inverted in support pedestal. The two tilt control knobs are shown.

Figure 3. The Ultra Tec machine with the precision polishing jig in place. Note the weights on the top of the jig.

Basic trigonometry is used to calculate the correction factor for the sample. The die is 6 X 6.6 mm which is roughly square, so we will assume 6.2 mm square for simplicity in this example. The thickness of the remaining silicon at points A, B, C, and D can be measured in lieu of the corner measurements made previously or calculated as an average from the adjacent corners. Example: thickness of silicon edge corresponding to side B = (AB+BC)/2 = 159 µm.

The remaining edges are calculated as: A=146, C=151.5, D=138.5. The angle between A and C is sin θ = opposite/hypotenuse. The die circuitry is considered the hypotenuse. The difference in height from A to D or B to C is the opposite leg of the triangle. The hypotenuse is the die dimension of 6.2mm. To correct the die tilt in the C to A direction take (C-A)/die dimension where the die dimension of 6.2 mm is converted to 6200 μm. The tilt correction sin θ = (151.5-146)/6200 = 0.89E-3.

Figure 4. Alpha Innotech Emission microscope setup with the precision polishing jig underneath. A laser illuminator is used to image the sample real time.

A 20 mm radius was arbitrarily selected from the center of the mount and marked at points A, B, C, and D. sin θ*20 mm = 0.0178 mm = 17.8 μm, therefore, an 18 μm adjustment is required to level the C to A direction. The C direction has more remaining silicon than the A direction so C is raised by 9 μm and A is lowered by 9 μm. Figure 5 shows the placement of the micrometer in order to adjust the tilt. The same is done for the DB direction. DB correction = (159 μm-139 μm)*20000 μm/6200 μm = 65 μm. Raise B by 65/2 or 33 μm and lower D 33 μm. The die view from figure 6 has 100 fringes from the center fringe to the left upper corner corresponding to an increase in silicon thickness of 15.5 μm.

Figure 5. Tilt correction with a micrometer.

Polishing to Target Depth

All that remains is to polish the silicon to the target thickness using a combination of 600 grit to 1200 grit sandpaper finishing with a colloidal silica polish. Focal depth measurements are used again to determine the amount of remaining silicon.

Interpretation of Interference Patterns

The interference patterns seen with monochromatic illumination allow an immediate view of the silicon thickness variance as shown in figures 6 and 7. Calculation of the film thickness variance is shown in Equation 3.[6]

$$(\lambda*OPD)/(2*n) = \Delta t \qquad (3)$$

n = index of refraction = 3.434 for silicon[7]
Δt = change in silicon depth.
λ = wavelength of light.
OPD = number of observed fringes.

Referring to figure 7, there are 36 fringes from the 30 μm label on the left to the lower right corner of the die. This corresponds to a change in thickness of 1.064*36/(2*3.434) = 5.6 μm. Focus measurements are used to determine the slope. In this case the edge is thicker by 5.6 μm.

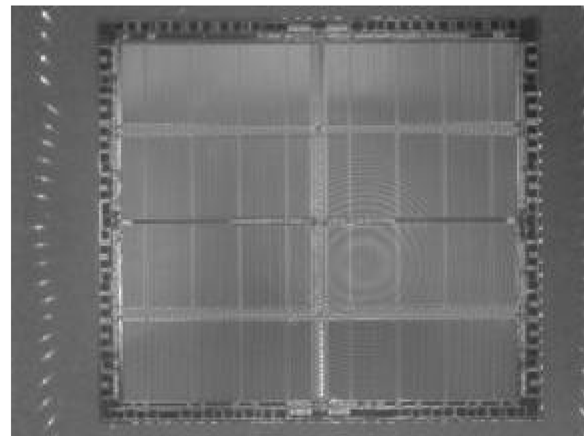


Figure 6. Interference pattern taken with a Mitutoyo 2X objective.

Wire to Wire Bonding

Since the silicon die is still embedded in the original package, the package acts as a carrier for the die. Depending on the nature of the package and die, the leadframe will be intact, partially polished or completely polished away. If the leadframe is intact, a probecard or socket can be used to establish electrical contact to the die through the remaining

leadframe or with wirebonding. If the leadframe is gone, the wires which are bonded to the die will be visible embedded in the plastic at the polished surface. Mechanical probes can be used to contact the embedded wires; however, the number of pins is usually a limiting factor to probes.

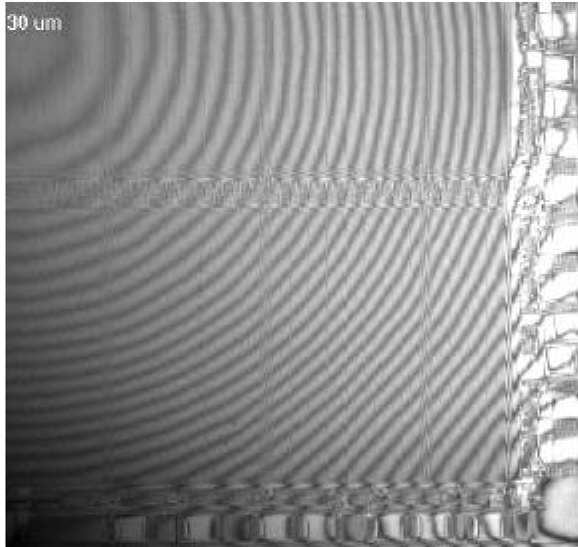


Figure 7. Interference pattern taken with a Mitutoyo 5X NIR objective.

Wafers can also be prepared for backside by dicing the wafer and wirebonding the die conventionally into an open leadframe or package. If an open leadframe is used it can be encapsulated with room temp epoxy prior to backside preparation.

Sizing the Chip

Polish the excess plastic material from the edges and thin the top if necessary being careful not to disturb the wire loops embedded in the plastic package. The polished chip embedded in the remaining epoxy can now be treated as an integrated circuit die. The embedded wires at the surface serve as bond pads and the polished backside is now considered the top surface as shown in figure 8.

Die Attach and Wirebond

The resulting part is attached to a new wireframe package and wire bonded to create electrical connections between the die and new leadframe. Figure 9 shows the die in place on the new package prior to wire bonding. Figures 10 and 11 are optical photos of a section of the finished product. The new pinout is implemented on the loadboard or a socket wiring adapter is used with the existing loadboard.

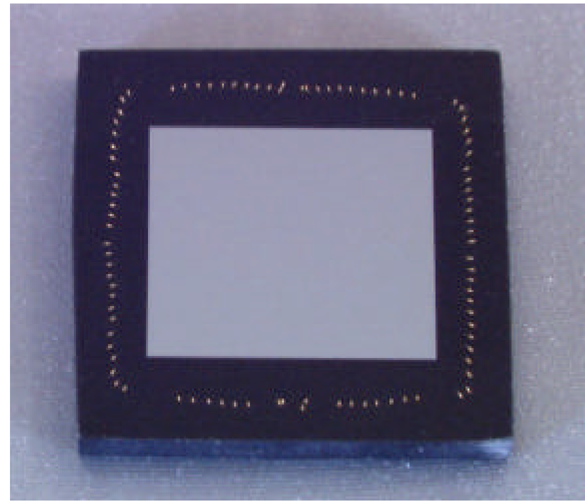


Figure 8. Original package after preparation.

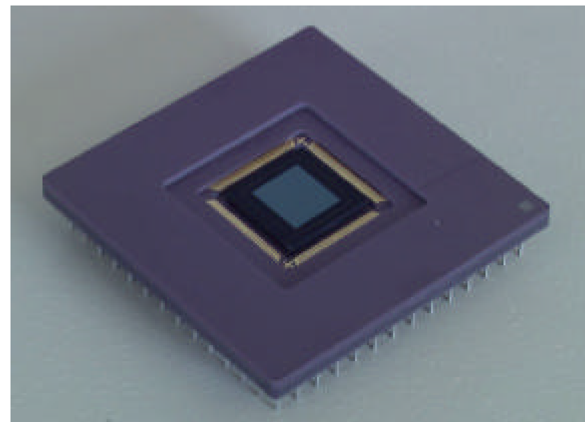


Figure 9. The sample is die attached with room temp epoxy to a 132 lead ceramic pin grid array and wire bonded.

Figure 10. Wire to wire bonds around the periphery of the package. The polished die surface is to the left.

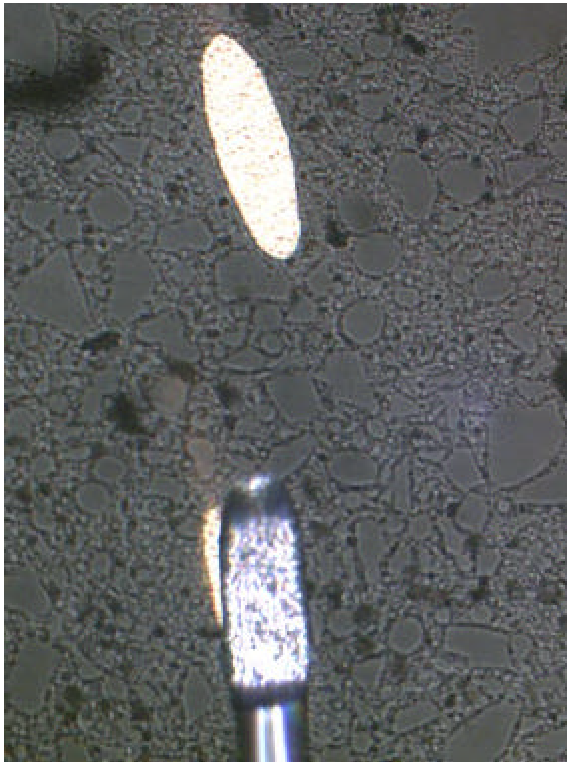


Figure 11. View of the wedge bond associated with one of 2 identical power pins. The other was left intentionally unbonded for illustration purposes.

Preparation on an Allied High Tech Polisher

As was done on the Ultra Tec machine another 100 pin PQFP Cache RAM was selected for backside preparation on an Allied High Tech machine. The part is mounted face down as shown in figure 12 and sanded with 400 to 600 grit carbide paper until the die is exposed. A 2 minute polish with 1200 grit sandpaper allows the part to be imaged from the backside for tilt planarization as shown previously. The method for tilt planarization is different for this machine but the fundamental concepts are the same. Note: The die size as a function of measured distance between the corners will be used (6 mm X 6.6 mm). Referring to figures 12 and 13, note the labeled areas. P is the pivot point which remains a constant. M1 and M2 respectively are the locations at which adjustable micrometer heads contact a spring loaded head. O is the opposing side from the pivot. Adjustment to M1 and or M2 allow tilt correction by affecting O relative to P and M1 relative to M2. As done previously, the thickness at the four die corners is obtained and averaged to find the midpoint thickness corresponding to points 1, 2, 3, and 4. The four corners of the die are imaged with the laser and the focal depth is measured from the surface of the silicon to the underlying circuitry. Pcorner = 212 µm, M2corner = 190 µm, Ocorner = 150 µm, M1corner = 176 µm. The correction is calculated as follows:

Calculate the midpoint values for 1, 2, 3, and 4.
Location 1 = (212 µm+190 µm)/2 = 201 µm.
Location 2 = (212 µm+176 µm)/2 = 194 µm.
Location 3 = (150 µm+176 µm)/2 = 163 µm.
Location 4 = (190 µm+150 µm)/2 = 170 µm.
Next calculate for the length of the opposite leg of the triangle from the pivot point P to M1 by taking the difference of location 1 to location 3. 201 µm-163 µm = 38 µm (.038 mm). This is the change in thickness across a distance of 6 mm. Doing the same for P to M2 = 24 µm (.024 mm) across 6.6 mm. All that remains is to calculate the amount of change required at M1 and M2 to planarize the surface. The fixed distance from P to M1 and P to M2 = 31 mm. Change M1 by (.038 mm/6 mm) * 31 mm = 0.196 mm. Change M2 by (.024 mm/6.6 mm) * 31 mm = 0.113 mm. The dial gauge is English so convert mm to mils and place the dial gauge under the polishing head as shown in figure 13. Set the dial to read 0 at point P and rotate the head to M1. Change M1 by turning counterclockwise the micrometer to obtain a change of 7.7 mils. Go to M2 and repeat using a change of 4.5 mils. Since the pivot, M1, and M2 are points directly under the micrometers, only one adjustment is needed. Confirm accuracy of the 3 locations and compensate the reading if required being sure the micrometer positioning is accurate. The remainder of the work is polishing to a target thickness. In this case 40 µm was chosen. Figures 14 and 15 are photos of the machine and polishing head respectively. Figure 16 shows the resulting interference pattern.

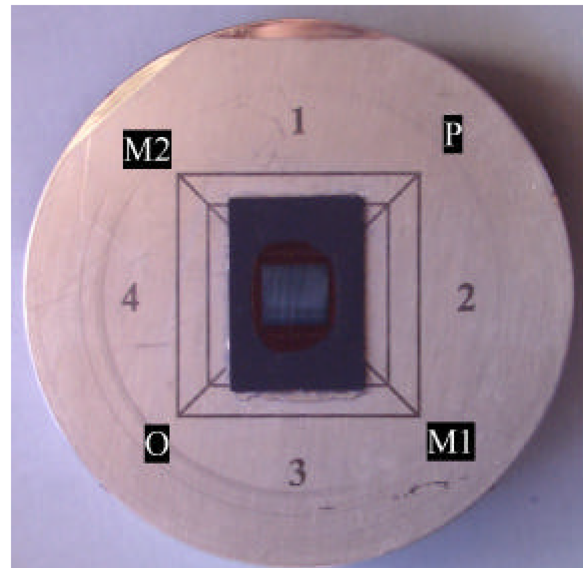


Figure 12. Mount fixture.

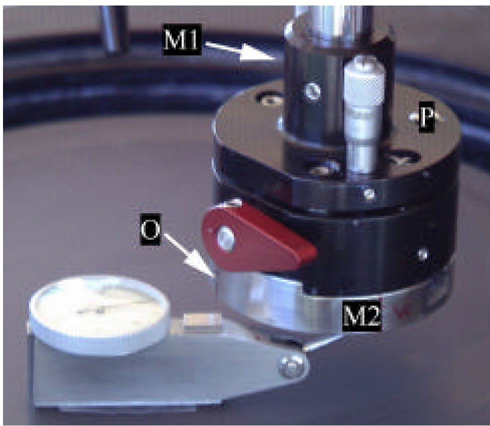


Figure 13. Tilt correction with a dial gauge.

Figure 14. Allied High Tech machine.

Figure 15. View of the polishing head.

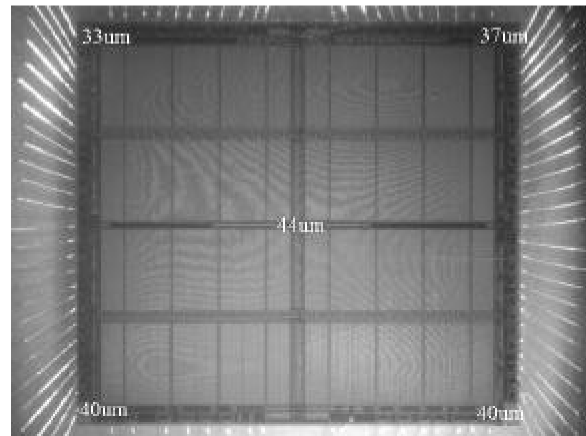


Figure 16. Interference pattern taken with a 2X objective. Thickness variations are shown.

The BGA and Chip Scale Package

Type 2A BGA packages cannot be prepared for backside analysis due to the location of the PCB and balls. Figure 17 shows three package types.[8] The type 2B and "Real chip size" packages can be prepared by mounting the ball side to the polishing fixture with a liberal amount of hot melt wax and polishing as described above. A more challenging package is shown in figure 18.[9] This package is a stacked design. Determination electrically as to which chip is failing dictates whether the SRAM or the Flash die is the polish target for wire to wire bonding. Figure 19 is the 3D multi-chip chip scale package.[10] In this configuration, if the lower die is the analysis target, then the package is prepared in the same manner as a type 2B. If the upper die is the target then the part is prepared the same as type 2A.

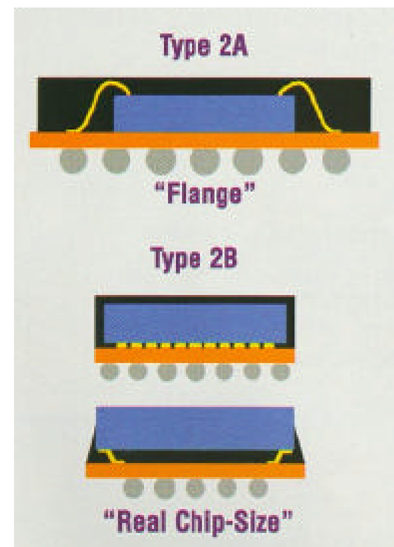


Figure 17. BGA Package types.

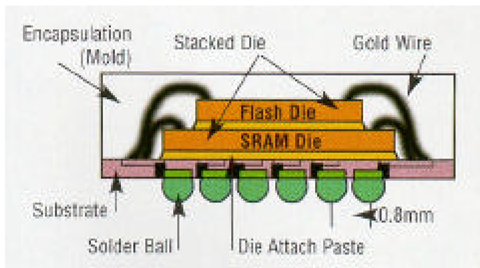


Figure 18. Chip scale package.

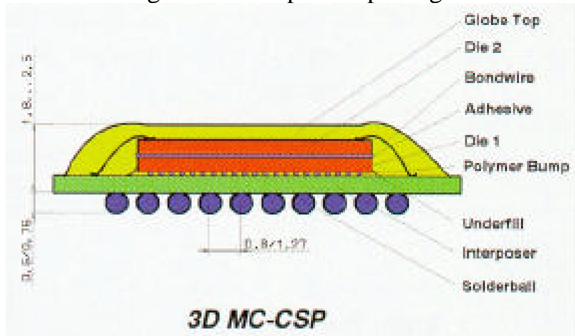


Figure 19. Schematic of CSP from MPD showing stacked chips.

Preparation of a Type 2A 312 BGA Package

Figures 20-22 follow the same preparation methods for the Ultra Tec polisher with a target of 20 µm thick. The balls and board are sacrificed. Once the target thickness is reached, the part is ready for wire to wire bonding into a new package. The outside dimensions in figure 22 are 15 mm X 15 mm. Figure 23 is a ring light illuminated image of the thinned die with the laser illuminator. The fringes are less pronounced if a ring light is used based on angle of incidence.

Due to the extremely thin silicon, shorter wavelengths of light can be used. Figure 24 is illuminated with a 940 nm infrared LED. Note the cloudiness of the image due to scattering in the silicon compared to figure 25 using the filter and bulb method of illumination.

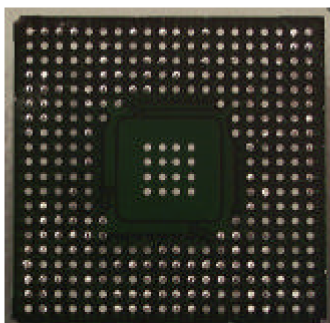


Figure 20. Ball side of Type 2A BGA.

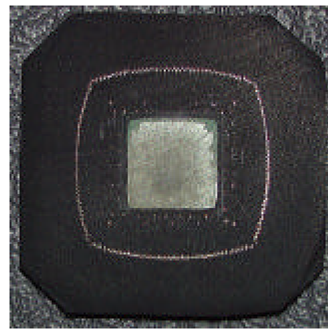


Figure 21. Balls and PCB sanded off.

With thin silicon, high magnification views of the circuitry is possible rivaling frontside images as shown in figure 26.

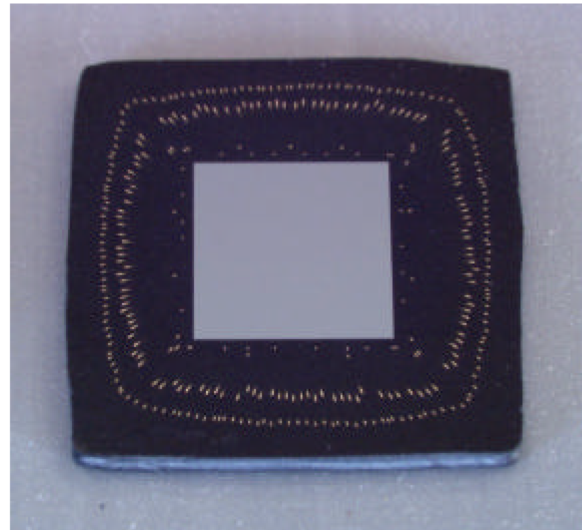


Figure 22. Polished BGA die in the original package ready for die attach and wire to wire bonding in a new package.

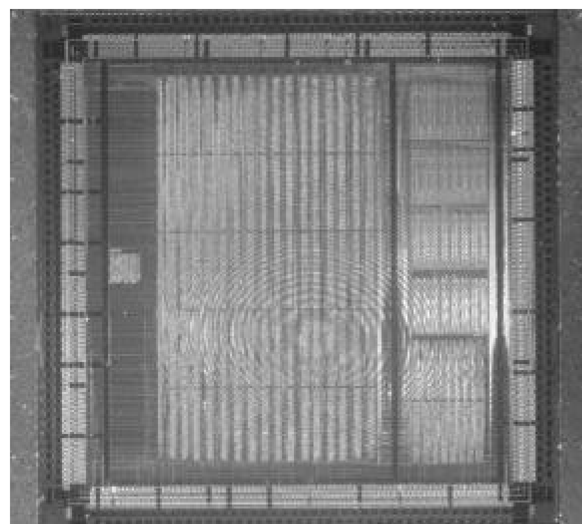


Figure 23. Ring light illumination 2X objective.

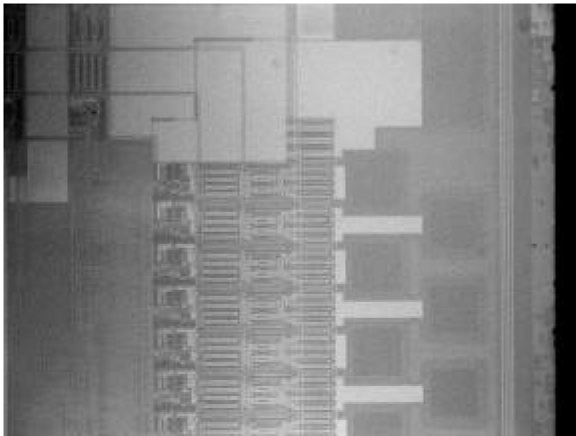


Figure 24. 20X NIR objective λ=940nm.

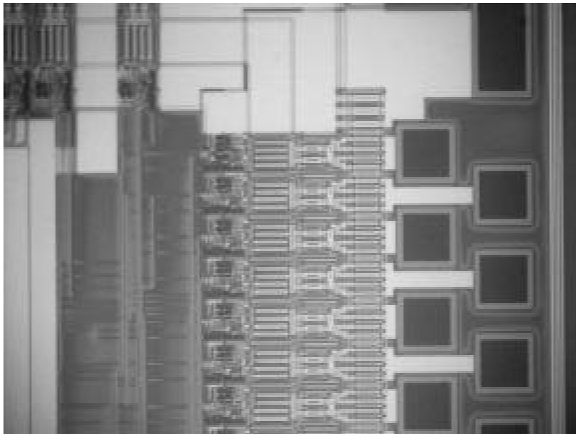


Figure 25. 20X NIR objective λ>1000nm.

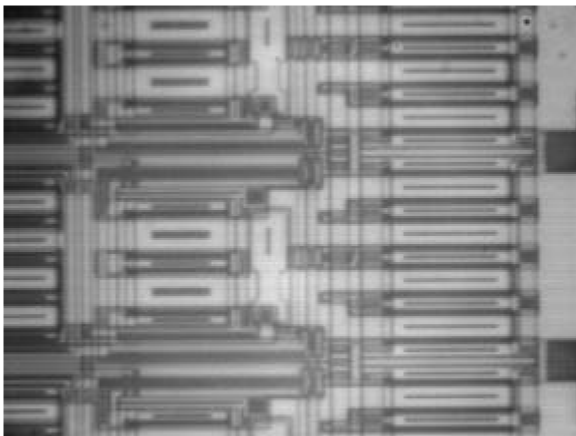


Figure 26. 100X NIR objective λ>1000nm.

Beam Vignetting

A great deal of hype has been generated over the years pertaining to numeric aperture (N.A.) and emission sensitivity especially regarding low magnification views. A publication pertaining to backside wafer level probing erroneously states that backside emission microscopy is "not achievable" without scientific grade fourth generation emission sensors.[11] Additionally, the paper references an application note identifying a macro lens with a numeric aperture of 0.4.[12] It is important to understand the relationship between Numeric aperture and f# in equation 4.[13]

$$N.A. = 1/(2*F\#) = n*\sin(\theta) \quad (4)$$

n = Index of refraction between the object and the microscope objective.
θ = The half angle of the cone of light entering the microscope objective.
F# = Effective focal length / lens diameter.

Numeric aperture defines the acceptance angle at which the microscope objective can transmit the light. Figure 27 is a ray trace model of a commonly used macro configuration with an alleged N.A. of 0.4. Note the configuration consists of two back to back f#1.2 camera lenses of which the lower lens is shown.

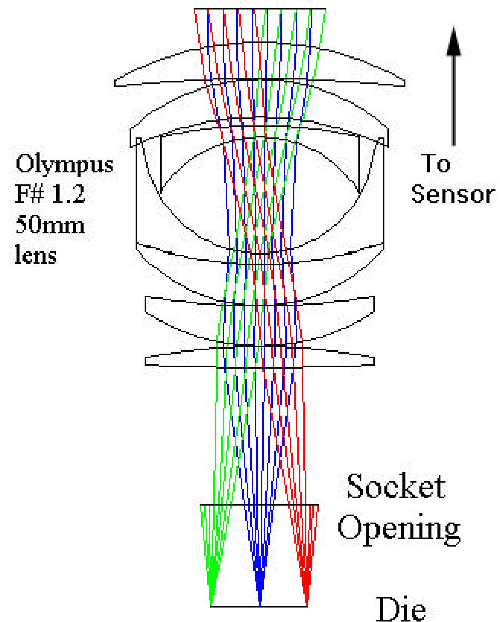


Figure 27. Ray trace model of macro lens configuration illustrating beam vignetting.

An f#1.2 lens= .42 N.A. only if the lens is used to view objects at infinity and project them on a 35 mm film plane. In the macro configuration, the lens elements are reversed resulting in drastically reduced N.A. The actual best case for this system is a 0.14 N.A. not 0.42 N.A. based on the ray trace model. A low N.A. lens does not necessarily mean it will be less sensitive. Since the depth of field increases with decreasing N.A., photoemission permeating in depth is more efficiently collected (such as saturation or forward bias) whereas localized emissions (such as a gate oxide rupture) are much easier to detect at higher N.A. values. Even though the N.A. is low, associated with the macro lens, the cone of light emanating from the device can still be obstructed (vignetted) by the socket hole and board in the traditional backside

configuration. The method shown in this paper eliminates both the working distance and beam vignetting issues.

Summary

A method has been shown allowing an integrated circuit, which is already encapsulated in a plastic package as well as individual die to be polished from the backside and electrically connected to a new package. The resulting orientation eliminates many of the problems of backside microscopy since the resulting package orientation is now frontside. Test equipment can be used in conjunction with analytical tools such as the emission microscope or focused ion beam due to the upright orientation of the polished backside silicon. It becomes obvious that this method can be used to intercept the electrical connection of a variety of package types such as Ball Grid Array, Pin Grid Array, PLCC, QFP, DIP, and SOIC to name a few. Flip chip technologies can be polished using the methods outlined above. Various surface probe and imaging techniques become viable from the backside due to the flat profile of the sample preparation such as:

1. Short working distance oil or water immersion lenses.
2. OBIC, LIVA, TIVA analyses.[14, 15, 16]
3. Thermal methods such as FMI and Liquid Crystal.[17, 18,19]
4. Backside chemical, FIB, and laser deprocessing.

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