REVIEW PAPER

ESD FAILURE ANALYSIS METHODOLOGY

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Abstract-This paper reviews Failure Analysis methods and discusses the merits and pitfalls associated with some of the more common techniques as they relate to ESD. Although advanced methods such as the Focused Ion Beam will be discussed, the importance of more traditional methods such as liquid crystal, emission microscopy, passive voltage contrast and mechanical polishing will be emphasized. Case histories are based on ESD related failure analysis; however, many of the references cover general Failure Analysis methodology.

INTRODUCTION

Published papers for Failure Analysis date back to 1954 for the Annual Symposium on Reliability and back to 1963 for the International Reliability Physics Symposium (IRPS). Another familiar resource to the failure analyst in the USA is the Symposium for Testing and Failure Analysis (ISTFA). ISTFA proceedings were originally known as ATFA (Advanced Techniques in Failure Analysis) and date back to 1974. The Microelectronic Failure Analysis Desk Reference is an important companion to the ISTFA Workshops.

IPFA (International Symposium on the Physical and Failure Analysis of Integrated Circuits) is another resource of information. The conference for IPFA has been held annually in Singapore for the last 6 years. ESREF is a European forum for reliability of electron devices, failure physics and analysis. ESREF held its first symposium in 1990. Additional resources of information are the Journal of Electrostatics, an Elsevier publication, ESA (Electrostatics Society of America), and IEJ (Institute of Electrostatics Japan).

The tools of the trade for the Failure Analyst evolve constantly. Some tools such as the Scanning Electron Microscope have endured the decades, whereas other tools such as the ultrasonic cutter were short lived due to the advent of the laser cutter and subsequently the Focused Ion Beam. The tools of the modern lab are a mixture of old and new. From the focused ion beam to mechanical polishing, each tool and technique has its place in the laboratory. The reader is strongly encouraged to review the references for a thorough treatise on the covered topics.

CROSS CORRELATION

Before forging ahead into an analysis, it is important to understand what failure test data is relevant. Resist the temptation to immediately jump on state of the art FA tools until the simple facts have been gathered. A report that omits supporting data and focuses on a single analytical method will be perceived as a weak report. The more exotic tools of FA must be used to reinforce or correlate the data for a sound corrective action whenever possible.

Since the path of an analysis is unique for each failure, consider each analysis step carefully before proceeding, especially, when unique failures are involved. If the mechanism is recurrent resulting in an abundance of samples, then cross-correlational methods are a requirement to a solid corrective action. The report the analyst generates must have sufficient supporting data in numeric and or photographic

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form to be believable to the reader. Since the written report is typically interpreted as the opinion of the analyst, document the data as a legal proof with sufficient supporting evidence. Try to generate the same damage on additional parts in order to support a corrective action. Analyze different parts with the same problem using multiple analytical methods. Arriving at the same result using differing analytical paths such as liquid crystal vs. Emission microscopy or cut and isolate techniques serves to reinforce the analysis. Recreating the damage (Simulation) with either HBM or CDM methods helps to identify whether the problem has more than one root cause. An example would be a poorly designed input protection scheme identified by damage to the gate oxide of the protected input. This example combines a design weakness with a CDM issue on the test floor.

Flowchart guides to failure analysis can be handy references, but lack the ability to teach common sense. Beware the analyst that goes to a 1-week course on electromigration and suddenly every failure mechanism encountered is due to electromigration.

LIQUID CRYSTAL

Liquid crystal analysis techniques actually have a rather lengthy history. Liquid crystal was first used for failure analysis of dielectric integrity as early as 1972 [1].

The next step for LC was its ability to map logic states of an operating IC somewhat similar to voltage contrast methods in the SEM [2].

Hot spot detection capabilities of liquid crystal were known since 1967 but weren't fully accepted as a practical tool until the early 1980's. Improved methods for cholesteric liquid crystals were used for hot spot detection in 1981 [3].

The current method of hot spot detection using nematic liquid crystal involves using a cross polarized microscope with K-18 liquid crystal from EM-Chemical Corp. Temperature control close to the transition point coupled with pulsed power is required to maximize the sensitivity of this technique [4].

Liquid crystal hot spot detection is commonly used to locate leakage due to ESD events and is inexpensive. Some problems with liquid crystal techniques pertaining to ESD analysis:

1. The liquid crystal pools around wire bonds and probe tips making identification of the hot spot difficult in some cases.
2. Temperature control fixturing adds overhead cost to the technique.
3. The number of layers between the source of the failure and the surface where the liquid crystal resides limits spatial resolution and sensitivity.
4. Liquid crystal has a set transition temperature. Multiple hot spots can be difficult to resolve if the "warmer" spot creates a significant temperature gradient.

FLUORESCENCE MICROTHERMAL IMAGING (FMI)

FMI is a thermal detection technique similar to liquid crystal but is implemented in a similar fashion to emission microscopy. FMI uses a rare earth compound (EuTTA) europium thenoyltrifluoroacteonate applied to the surface of the die in a similar manner as the application of liquid crystal. The techniques differ in that FMI converts the blackbody radiation of the sample into visible light (under ultraviolet excitation) which decreases with increasing temperature. A comparison image is created from the die at ambient by image subtraction of the unbiased condition from the biased condition. Local thermal differences appear due to the difference in generated visible light associated with the region of interest. While the technique is an order of magnitude more sensitive than liquid crystal (.01C), it is also orders of magnitude more expensive to implement. FMI is a good technique due to both spatial resolution improvements and thermal detection improvements [5,6].

EMISSION MICROSCOPY

Emission Microscopy began as infrared emission microscopy and was used originally to image near infrared energy emitted from CMOS latchup sites [7]. Since this technique images the light emitted from the latchup site, multiple latchup sites could be observed and the propagation of the effect characterized to enable debug. This method of imaging was proven to be superior to liquid crystal for latch up analysis due to the ability to spatially resolve multiple sites irrespective of a transition temperature.

The next and rather significant step for emission microscopy was directly related to ESD protection structures. Using a transmission line pulse setup in conjunction with an infrared-viewing microscope allowed ESD related design to take a leap forward. A dynamic visual understanding of where the energy was going and how it was being adsorbed for varying pulse energies allowed models and rules to be created for ESD design [8,9]. An explanation of the non-uniform conduction in avalanche of an n-channel and subsequent weakness was derived compared to a p-channel device as follows:

1. Hot electrons are injected into the gate oxide locally (positive drain voltage) associated with the avalanche event. These hot electrons are responsible for the reported "lock on" effect which generates a non-uniform region of current flow. The local trapping of the electrons generates a local pinch-off in the channel. The resulting high local electric field acts as a positive feedback effect, which reduces the effectiveness of the n-channel protection.
2. Conversely, the p-channel device reduces the local electric field (negative drain voltage) at the avalanche site making the device stable and capable of dissipating much higher energies.

Wider pulse widths (120 ns) were reported to result in gate melting and contact spiking effects due to localized heating of the silicon (second breakdown effects).

As stated by the authors of this technique "EOS/ESD analysis will cease to be black magic, but will be transformed into a science." Transmission line pulse methods are a common tool today coupled with emission microscopy [10-13].

EMISSION MICROSCOPY AND GATE OXIDE DAMAGE

Emission microscopy of CDM created low level gate leakage (Latent ESD) requires a considerable improvement in emission microscopy [14,15]. Once leakage has been identified associated with an input gate, the gate can be analyzed to determine the number of leakage sites associated with that structure as well as the magnitude of leakage at each site. Device geometry in this example was such that a major power buss was positioned over a section of the input gate and the emission sites were located under the power buss. For this reason, the passivation surface was cracked gradually with a mechanical probe and metal etch was used to remove the power buss over the input structure. The Focused Ion Beam (FIB) can also be used to open the buss. The leakage of the input was confirmed to remain reasonably constant around the 100 nA range at 5V.

Emission microscopy was performed and two emission sites associated with this one particular input pin were identified. The bias voltage was 10V. The reasons for this high bias voltage were that no emission sites could be identified at lower voltage ranges and this voltage value was prior to any permanent damage being done to the gate. The two emission sites had varying intensities as seen in figure 1.

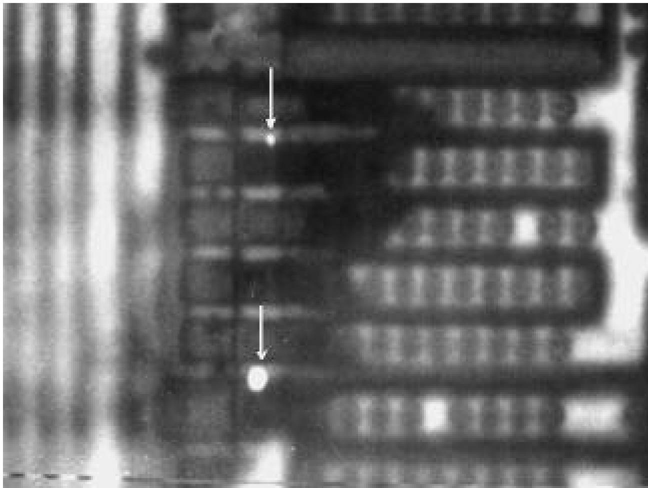

Figure 1. Two emission locations were identified on the input gate responsible for 110 nA of leakage at 5 Volts. The drive voltage was 10 volts with a CCD acquisition time of 400 seconds.

These emission sites correspond to the leakage associated with each finger. This emission image was taken with a Zeiss Confocal Laser Scanning Microscope and a CCD cooled camera. The CCD cooled camera was utilized with an integration time of approximately 400 seconds and noise averaged for this image to be observed. (These are extremely low-level emission sites). Most intensified based emission microscopes, and certainly the older infrared microscopes, are incapable of detecting such a low-level signature of photon emission. This device was first deprocessed to expose the polycide and then each polycide finger was laser cut over field oxide to sever the individual fingers from the common polycide connection. The two edge fingers were mechanically probed and observed to leak, corresponding to the emission photograph (Figure 1). Using a curve tracer set in DC mode at 5V, leakage on one finger was approximately 70nA, and 30nA on the other finger. Notice this corresponds roughly to the intensity of the emission sites from figure 1 and equals the measured value of the leakage identified prior to deprocessing.

THE OPTICAL MICROSCOPE

Of all the tools available to the analyst, the optical microscope is used routinely throughout the analysis process. Optical microscopy has several modes of operation:

1. Brightfield imaging uses light which is coaxial through the objective and is the common mode for imaging opaque surfaces.
2. Transmission mode is commonly used for transparent specimens mounted on glass slides. This mode is commonly used for biological specimens.
3. Darkfield imaging illuminates the sample at an angle. The resulting image reveals elevated surface topography due to the scatter of light off of the edges of the elevated surface. This method is commonly used for surface contaminant identification.
4. Interference contrast or Nomarski is used for the identification of subtle surface morphology changes. Profile changes such as a thin film boundary are seen as a color change. Cross polarizers with a wedge analyzer are used in this mode.
5. Laser confocal microscopy allows 3D reconstruction of surfaces for defect profiling. Laser based microscopes allow features to be identified and characterized based on the laser wavelength.
6. Spinning disk confocal microscopes generate a similar effect to the interference contrast mode but with much greater depth of field and on entirely different principles. Objects, which are out of focus, are also attenuated proportionately in brightness. Objects, which are in focus, appear multicolored depending upon the surface morphology.

Additional information on comparative data for optical microscopy can be found in the supplied references. [16-18]

THE SCANNING ELECTRON MICROSCOPE

The SEM has been a major part of failure analysis laboratories since the 1960's. The SEM is used to image as well as probe. Detectors associated with a SEM allow information to be gathered from conductor potential to elemental analysis of materials. Numerous probe methods have evolved associated with the SEM [19-21].

Secondary electron detection is the most commonly used mode for the SEM. This mode allows surface morphology to be ascertained due to the high resolution coupled with a large depth of field. The SEM is a surface imaging tool and cannot image effectively through oxides compared to an optical microscope. Electron beam charging of insulators can be problematic and is typically addressed by using a few nanometers of a sputtered conductive coating such as carbon or gold. The references in this section provide a thorough treatise on SEM techniques.

PASSIVE VOLTAGE CONTRAST

Another method of analysis, which can be used to identify gate leakage, is Passive Voltage Contrast (PVC). [22-27]

This analysis method allows non-contact identification of gate leakage in the Scanning Electron Microscope. PVC will identify any floating nodes on an IC. In order to observe input gate structures, the gate must be electrically disconnected. Any leakage path to substrate will be seen as a contrast difference from the surrounding field oxide. Applications of this technique allow identification of gate leakage as well as identification of any floating connections such as metal. In the previous section, a part, which had leakage due to CDM stress, was analyzed using emission microscopy. In this section PVC methods coupled with the laser cutter will be shown. The input leakage, in this case, was measured at 99 nA prior to any deprocessing. Passivation and metal were first removed, and BPSG was thinned over the polycide with HF acid. (Note that PVC could be performed at this point by imaging the exposed contact windows.) The polycide gate was then exposed in a Technics RIE 800 etcher with CHF_3 at 6 SCCM (Standard Cubic Centimeters per Minute) and O_2 at a 1 SCCM flow rate. Five minutes at 150 watts was typical for removal of the remaining oxide layer.

The prepared sample was appropriately grounded at substrate and placed in the SEM at 2KV accelerating voltage and 60° tilt. No electrical feedthrus or fixtures were required since the electron beam provided the bias. Figure 2 is a SEM PVC image of the gate leakage. The illuminated gate structure leaks to substrate. Since the electron beam provides current to substrate in the sub-nanoamps range, the gates will not be damaged. SEM inspection at 10 kV and then PVC at 2 kV is typical, and will not alter the leakage performance if the beam current is not excessive.

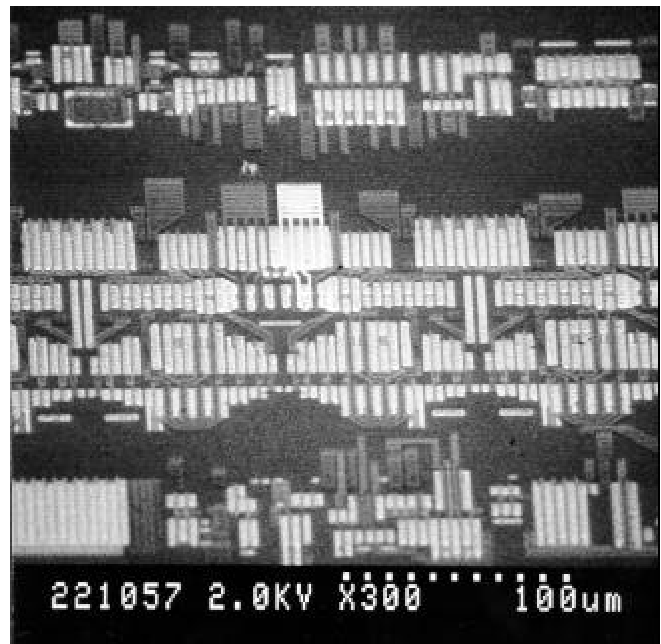

Figure 2. SEM PVC image which shows gate leakage associated with the first input inverter. The failing gate structure in the center is illuminated.

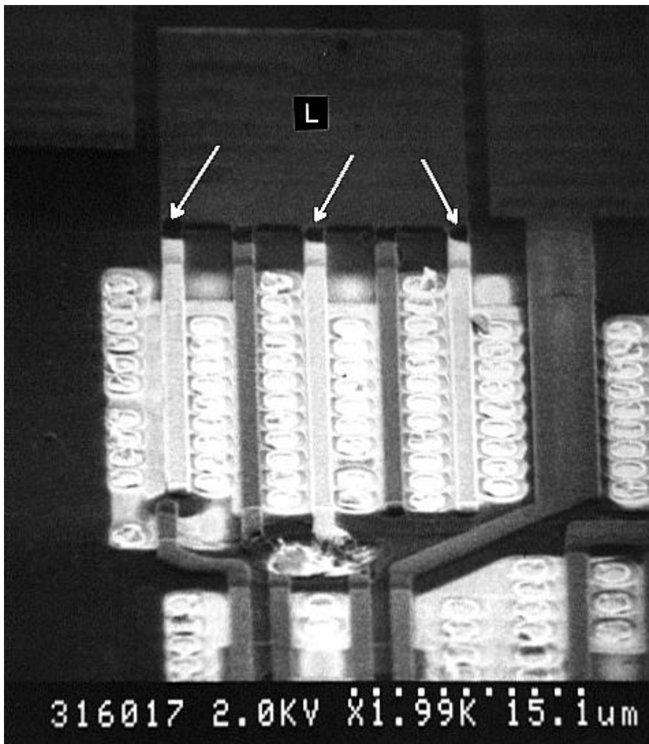

Figure 3. SEM PVC image which shows latent leakage on the two end fingers and the middle finger of the Laser isolated input structure. This gate is labeled "L".

The input leakage is actually a sum total of several leakage paths to substrate associated with a failing pin. The five individual input gate fingers of this latent input leakage were laser isolated over field oxide and imaged with PVC as shown in figure 3. After imaging, the five isolated fingers were mechanically probed with the following results:
Leg 1=42 nA, leg 2=0 nA, leg 3=41 nA, leg 4=0 nA, leg 5=16 nA
Total = 99 nA. This value equals the measured value of the leakage identified prior to deprocessing.

The advantages of PVC are:
1. Allows rapid identification of gate oxide leakage at low magnification while scanning across thousands of isolated gates.
2. Detects any floating nodes such as discontinuous metal connections.
3. Reveals presence of thin oxides over a conductor such as incomplete bond pad etch resulting in poor ball bond adhesion.

The disadvantages of PVC are:
1. Requires the suspect area to be exposed (free of oxide) either at metal, contact, or gate.
2. Requires the suspect area to be isolated. Gates which employ buried contacts will appear as gate leakage failures due to the buried contact connection.

THE FOCUSED ION BEAM (FIB) AND LASER CUTTER

FIB milling was first used to polish samples for the Transmission Electron Microscope (TEM). The FIB has evolved significantly and is commonly used today to electrically isolate metal and poly interconnects as well as reroute them. The FIB is also capable of cross sectioning and imaging a select area. Defects such as step coverage or interlayer shorts can quickly be identified with the FIB. Generally speaking, the FIB is a microsurgery tool which allows metal and or oxide to be removed or deposited [28].
The FIB is an imaging tool similar to the SEM and therefore beam related interactions such as voltage contrast are present [29].
The FIB is currently the most expensive tool in a Failure Analysis lab, which makes time on a FIB precious. Caution must be exercised when using a FIB to isolate a gate structure. The beam current of the FIB will generate a significant tunnel current in the gate oxide if precautions such as a flood gun are not used. A FIB operator that understands the pitfalls can cut and connect just about anything on an IC without detrimental impact.
The Laser cutter has evolved from NIR energies of 1064 nm to UV energies of 355 nm. Current systems use a Nd:YAG pulsed laser with selectable frequencies and a definable aperture size. The laser cutter is useful for rapid removal of material especially polyimide whereas the FIB

is not great at removal of polyimide. Windows in passivation can be opened where nitride materials are involved and metallization can be vapor deposited with a laser [30]. The laser is faster but not as precise or repeatable as the FIB. Beam charging effects are not an issue with the laser cutter making it a good choice for in situ cut and isolate techniques.

DELAYERING AND STAIN ENHANCEMENT

Delineation of layers or defects dates back to 1955 when W.C. Dash developed what is known as Dash etch today. Dash etch is a HF-HNO_3 system currently used for p-n junction delineation. Other etchants such as Sirtl etch are based on a HF-CrO_3 system. Sirtl etch delineates defects such as stacking faults and dislocations in silicon. Sirtl etch has excellent wetting properties and works well as a poly etch for revealing dielectric integrity issues in the MOSFET channel. Wright etch is an improved version of Sirtl etch with nitric acid and copper nitrate combined in the HF-HNO_3 system. Wright etch is commonly used for damage enhancement in ESD analysis. There are currently thirty-eight additional etch formulations which should not be ignored. An excellent resource for etch delineation as well as deprocessing recipes and references was recently published by T.W. Lee in 1996 [31].

SURFACE LAPPING TECHNIQUES

Sample preparation is straightforward and a few guidelines will result in repeatable clean results. Use high selectivity etches such as KOH or CsOH to insure an endpoint on the point of interest. Other etches include 49% HF, or metal etchants. Etches which are not highly selective such as a poly etch containing nitric and HF, will not leave crisp definition associated with silicon to oxide boundary and will, in many cases, remove too much gate oxide. Mechanical surface lapping techniques allow layers to be partially exposed and then removed using a selective etch. In order to expose the gate oxide of a failing transistor to examine the gate oxide integrity topographically, the following procedure is employed:

A. Surface polish the part using 1 micron diamond mylar lapping film or if planarity needs to be maintained use a napless cloth with colloidal silica such as chem-pol on an orbital polisher. Once the oxides over poly 2 are eliminated, use HCl to remove the silicide then heated KOH to remove the exposed poly surface. Endpoint is determined empirically. The etch will endpoint on the gate oxide with a 200:1 selectivity and remove any silicon radially under the defect. High oxide sidewalls will be seen which may interfere with imaging in the Atomic Force Microscope AFM due to tip convolution. The sample can at this point be stripped of oxide using HF and the substrate or poly 1 cells imaged as desired. Surface lapping eliminates etch undercut and artifacts common with traditional delayering and is useful for AFM as well as SEM imaging.

SELECTING THE RIGHT TOOL FOR THE ANALYSIS OF ESD FAILURES

As a general guideline, emission microscopy is a poor choice when dealing with ohmic leakage such as ESD damage to a contact or junction. Typically most of the energy liberated is best detected using a thermal detection technique such as liquid crystal or fluorescence microthermal imaging (FMI). Emission microscopy is usually the best choice when dealing with damaged gate oxides or junction related phenomena. Since transmission pulse methods result in amps of current flowing through the protection structures in a repetitive mode, it is clear that sensitivity is less an issue where design verification is involved. All emission tools of today, be they CCD based or intensified systems, offer orders of magnitude sensitivity gain over the original IR imaging methods which used an S-1 photocathode (Gain = 10X).

Cut and isolate methods to isolate leakage can be performed with the laser cutter, FIB, or by

mechanical probe. Caution needs to be exercised where fragile gate oxides are involved due to possible beam charging in the FIB.

THE FUTURE OF ESD FAILURE ANALYSIS

Atomic Force Microscopy (AFM)

The AFM is rapidly coming of age. The AFM can image with resolutions of 1 angstrom in all three axes. Coupled with imaging modes such as capacitance probe, junction locations can be identified and dopant variations identified in both cross sectional and topographical directions. The integrity of dielectrics can be mapped using tunneling AFM. Current flow can be mapped in the low microamp range with magnetic force modes and Electrostatic force mode can map local electrostatic surface to tip interactions [32].
Figure 5 is an AFM view of a damaged gate oxide due to a CDM event. Note the cone shaped hole. This is due to tip convolution as the edges of the tip enter the hole. The edges of the hole were measured to be: Y = .19 μm, X = .14 μm. Notice that the etch undercut ring from figure 4 is not visible in the AFM image since the AFM reveals the true surface profile. In cases such as this, ultrasonic cleaning must be avoided die to the fragile nature of the gate oxide rupture. The AFM will image this oxide without damage in tapping mode.

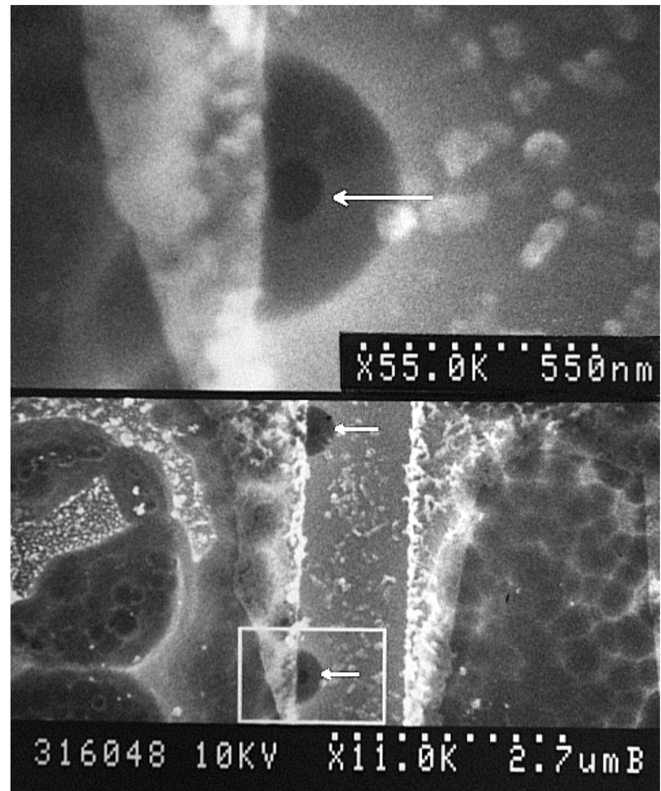

Figure 4 SEM high magnification split view of the CDM damage sites. Note the hole within a hole. The outside dark ring is due to plasma undercut that removed the underlying channel radially from the rupture. The size of the rupture ranges from .15 μm to .26 μm in the Y direction and from .12 μm to .19 μm in the X direction for various samples.

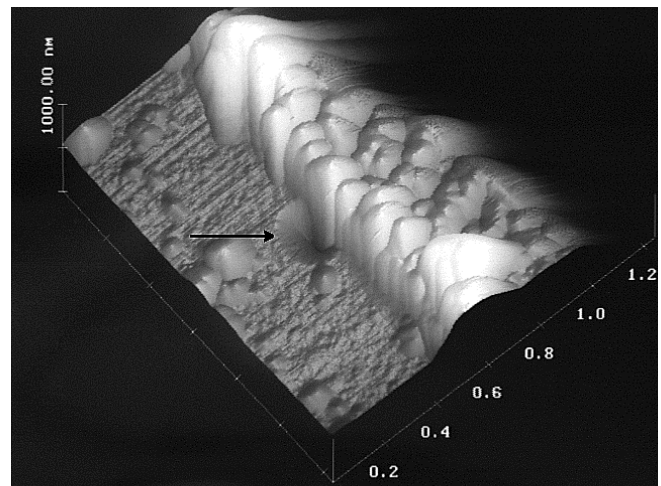

Figure 5 Atomic Force Microscope image of the CDM damage site. Compare the appearance of the oxide sidewall to the SEM image in figure 4.

Backside Emission Microscopy

Backside Emission Microscopy is rapidly becoming popular and could be used with transmission line pulsing techniques, however, the effects of thinning the substrate must be taken into account.

Backside emission microscopy simply refers to performing emission microscopy imaged from the polished and thinned substrate of the device [33-40]. Backside emission is used due to the number of metal layers blocking a clear view from above.

There are several significant challenges associated with backside emission microscopy:

1. Sample preparation methods.
2. Thinning the substrate will impact device characteristics. The device will have reduced thermal and electrical conduction transport characteristics and an increase in the parasitic gain for latchup where low ohmic substrates are involved.
3. Silicon is an infrared filter and limits detection bandwidth of emission sites.
4. Dopants in the silicon serve to scatter NIR energy resulting in attenuation of sensitivity.
5. CCD based systems have a low quantum efficiency in the required NIR spectrum.

To date, there are no published papers on backside emission microscopy associated with ESD failure analysis. Overlying metal which blocks the field of view such as a power buss is typically removed by opening a window to allow a view of the underlying structures from above. There is a great deal of emphasis on backside emission microscopy and a corresponding quantity of misinformation from some of the vendors of these products. None of the CCD camera manufacturers publish data on quantum efficiency at or above 1000nm. The data is typically extrapolated to 1000nm and cannot be relied upon as an absolute measure. Keep in mind the limitations 1-4 cited above. Technology limitations of item 5 is best illustrated by generating a bandpass curve of CCD response to broad band energy from a quartz halogen bulb filtered through a polished silicon filter. The wavelength is selected with a monochromator calibrated for the NIR spectrum. From figure 6, 1036 nm and 1117 nm are the half bandwidth or 50% intensity points with 1073 nm at the center. This data will shift as much as 100nm toward the visible depending on the thickness of the silicon filter (item 2) but it is clear that discussion of back thinned CCD sensors for UV and visible quantum efficiency improvements are irrelevant in this area of the spectrum. It is prudent to compare a known back-thinned sample under a known bias condition in order to evaluate the backside technologies on the market.

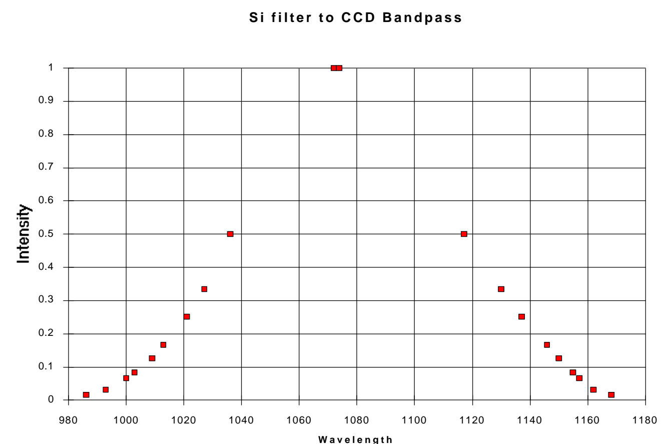

Figure 6. CCD sensor to silicon filter response.

ESD FAILURE ANALYSIS HISTORICAL REFERENCES

An excellent reference for the relationship between HBM events, CDM events, and the associated damage mechanisms in silicon was written by B.A. Unger IRPS 1981 [41].

A source guide for failure trait photographs can be found in IRPS 1982 [42]. This source guide is from a workshop report that contains a reference table of photographs and the related failure mechanisms.

A discussion on thermal runaway commonly known as second breakdown can be found in ISTFA 1984 by Middendorf and Hausken [43]. This paper covers the following failure mechanisms: Junction damage, gate oxide damage, poly filaments, aluminum melt filaments and fused open conductors.

A study of CDM failures for input and output structures for two different designs can be found in EOS/ESD 1994 by N. Maene et al. [44].

J. Never and S. Voldman used the AFM in conjunction with the SEM to show subtle differences in surface morphology after second breakdown damage in EOS/ESD 1995 [45].

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