Functional Failure Analysis by Induced Stimulus

Jim Colvin
Consultant
36217 Worthing Dr.
Newark, CA 94560
(510) 851-5555
E-mail: jbcolvin@pacbell.net

Abstract

In the field of failure analysis of integrated circuits, diagnosing functional failures is a requirement. Traditional beam-based analysis techniques use a scanning laser or e-beam to induce a parametric shift which is monitored through changes in current or voltage driven to the device. Deep submicron technologies frustrate these analytical methods due to the nearly immeasurable parametric shifts externally caused by a small signal leakage path internally. These internal failures can be identified functionally by timing, temperature or voltage dependencies but the exact location of the fault is difficult to isolate. RIL (Resistive Interconnect Localization) is a newer technique which can identify via anomalies functionally using induced thermal gradients to the metal but does not address how to uniformly inject the thermal energy required in the silicon to analyze timing design deficiencies and other defects.[1] With SIFT (Stimulus Induced Fault Testing), numerous stimuli will be used to identify speed, fault, and parametric differences in silicon. The heart of this technique revolves around intentionally disturbing devices with external stimuli and comparing the test criteria to reference parts or timing/voltage sensitivities. Synchronous interfacing is possible to any tester without any wiring or program changes.

SIFT Scanner System

The concept began with the author back in 1986 by placing a pinhole in aluminum foil to reduce the illumination spot size on a B+L optical microscope on a probe station and manually rastering the spot over the device under functional test.[2] A looping test pattern went into failure as the spot was scanned over the defect. This technique was also used parametrically with a curve tracer to localize and confirm the defects during the stripback process.

The SIFT scanner does not use traditional laser scanning microscope optics and is actually quite straightforward in construction. DUT scan area can be microns to 12" or more, allowing whole boards, packages and die to be analyzed since the scanners are stepper-based rather than internal optics based. Field of view limitations of objectives on LSM (Laser Scan Microscope) based equipment are eliminated with SIFT. Data output is to a PC via multiple RS232 channels and contains data from the scan for X, Y, and multi-channel data for each step in the scan. This data is coordinate data but can also be displayed photographically in .raw format using Adobe photoshop at present. Channel data consists of pass/fail signals from the tester as well as analog information. The scan and step is user defined based on spot size.

The system can be based on either a motorized probe station or microscope stand for test head applications. Unlike LSMs, SIFT uses a stationary beam and moves either the stage or the microscope head in a raster scan pattern. Figure 1 is a block diagram of the apparatus. A microscope and stage are equipped with stepper motors to control the X, Y, and Z motion of the scan. Obviously servo motors or similar linear positioning devices can be used in place of stepper motors. Z control is necessary to control the spot size of the stimulus by either focus or proximity control of the source. Laser based SIFT uses a laser attached to the top camera port of the microscope and can be any wavelength compatible with the selected optics. The selected objective, aperture, and focus control spot size, in this case.

CO2 lasers can be mounted in place of the microscope and raster scanned over large areas for thermal SIFT. The stimulus can also be introduced over the DUT with the raster applied to the stage. This method of SIFT can be thought of in the same way a probe is positioned over a DUT by moving the stage.

The microcontroller is based on a Microchip Inc. PIC17C756 and runs over 1500 lines of C code to handle all the required functions. The microcontroller handles X-Y-Z positioning, stimulus, and communicates with the tester. Communication can be synchronous, where the microcontroller will step only after receiving pass/fail from the tester or handshake with the tester, for multi-loop platforms. In this paper, the synchronous mode is used to demonstrate interfacing to the tester without any electrical connections via phototransistors. It should be apparent that direct connection means are also possible.

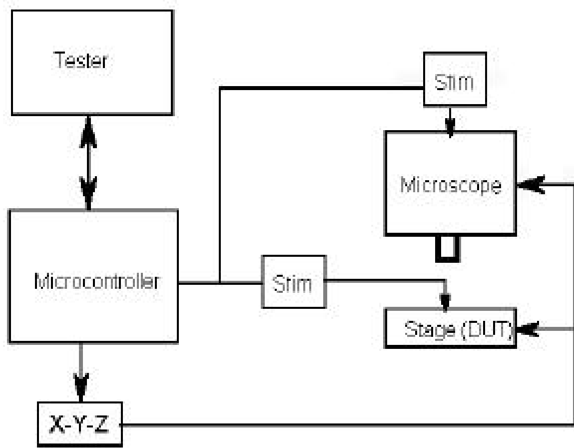


Figure 1. Block Diagram of SIFT Scanner.

Stimulus Methods

Optical Beam Induced Current

The setup to obtain an OBIC (Optical Beam Induced Current) image using SIFT will allow a comparison and facilitate an explanation of the scanner. Traditional OBIC uses a LSM and a current detection amplifier to sense and display photocurrents induced by the laser.[3] SIFT is implemented by either using the current detection amplifier or by interfacing a curve tracer to the analog signal input of the microcontroller. The curve tracer X and Y internal amp signals are wired to the microcontroller, allowing the curve tracer to handle the scaling while the X and Y outputs supply .5V/division signals. The curve tracer spot positioning serves to set the offset to the microcontroller. The advantages of this method hinge on being able to monitor I-V relationships rather than only constant voltage or constant current methods.

The overlay image or photograph also needs to be obtained. One method is to scale an optical image or layout to the scanned image since the scanned image has exact coordinates for the scan compatible with layout information. The other method is to create the image by sampling the reflected light from the laser during the scan in a similar manner as the LSM. The laser source is a 670nm laser diode, which is focused to the diffraction limit (smallest spot size), for the scan. The detector is a phototransistor linked to the microcontroller with an adjustable gain. The 30 frames/second CCD camera and LCD monitor allow navigation as well as the ability to serve as a photodetector port. The user may insert the photodetector in the microscope path in place of an eyepiece or similar port for reflected light sampling or the photodetector could be affixed to the LCD screen associated with the CCD image. This method works so well that it is the preferred method. A settle time of 40 msec is used at each sample location for the LCD display-based detection. Although this may seem slow compared to traditional OBIC techniques, most applications have significant capacitance, especially decoupling at Vdd. Control of the scan sample rate is important based on the device parameters for settle time. Figure 2 is an OBIC image obtained with the curve trace interface and the photodetector affixed to the screen. The microcontroller runs the scan based on input parameters. The step is set to 3 um, which means that the microcontroller will stop every 3 um and sample the OBIC signal and reflected laser signal simultaneously. The scan area is determined by simply setting the origin and navigating with the joystick +X and +Y to define the scan area. The display shows how large, in pixels, the photo will be as well as the pixel size in microns. Upon initiation, the scanner will raster scan until coordinate 0,0 is reached. The resulting data files can be viewed in CSV (Comma Separated Values for a Spreadsheet) or raw (photoshop) formats depending on the preference. The spot size for the stimulus can be different than the spot size for the background image, unlike an LSM system.

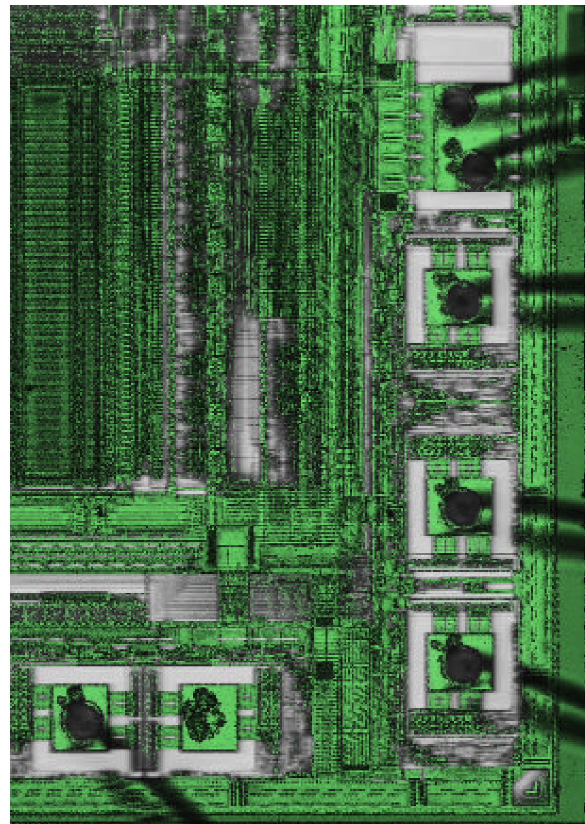


Figure 2. OBIC SIFT image of Vdd to Vss. 305x435 pixels with 3 um pixel size.

Electrical Biasing

Many different ways to electrically bias the sample for beam based measurements exist and all are compatible with SIFT. LIVA (Light Induced Voltage Alteration and TIVA (Thermally Induced Voltage Alteration) use a constant current source to facilitate

measurement of impedance.[4,5,6] OBIC and OBIRCH (Optical Beam Induced Resistance Change) use fixed voltage sources and monitor current.[7] XIVA (Externally Induced Voltage Alteration) uses an inductor and monitors developed voltage similar to CIVA (Charge Induced Voltage Alteration), LIVA, and TIVA.[8] A serious disadvantage to biasing with a constant current source is the risk of overvoltage due to the non linear nature of the turn on point for semiconductors. The author prefers a series resistance divider method for signal generation. The voltage developed on the series resistor is varied to develop a desired drop voltage to the SIFT amplifier. The current detection gain of the divider is determined by the chosen resistor value and current drawn by the IC. Resistors have no bandwidth limitations compared to the active current source. XIVA signals are dependent on the timing of the event signal and the chosen inductor.[9]

An active circuit useful for supplying constant current type performance with constant voltage control is described in figure 3.[10] The circuit consists of a voltage controlled constant current source, which is used to drive a constant current across the DUT. The resulting voltage drop across the DUT is buffered at J2 and supplied to a lowpass filter. The lowpass filter supplies the DC value of the DUT bias to a summing circuit which adds the negative desired set-point of the DUT (Compliance voltage set-point) to the actual measured DUT bias. The result is multiplied by -2.7 and used to control the dependent current source such that Vcc is maintained on the DUT. The signal at J2 is also supplied to a high gain active filter for detection of the ONS (Oxide Noise Signature) signal. The ONS signal is monitored during a SIFT scan to identify minute shifts in operation during a scan.

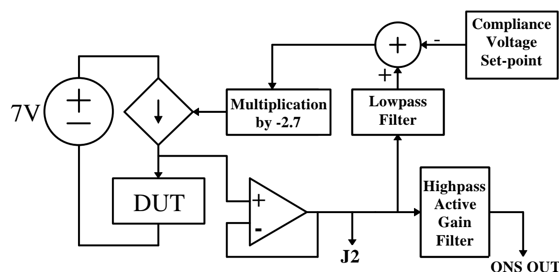


Figure 3. Block diagram of the ONS circuit.

RF Stimulus

RF SIFT uses an RF probe tip to either inject or receive RF energy over the DUT. This technique is useful for board, package, and die level to trace circuit paths carrying the characteristic frequency. Opens can be identified assuming the capacitive coupling across the open is not dominant. Spatial resolution and signal strength are impacted by proximity of the DUT to the source as well as tip geometry. Frequency is selected based on the amount of capacitive coupling desired between the tip and source. The tip is normally the sensor with the trace biased at the desired RF frequency. As with any electric field based method, the conductor of interest must not be shielded. Figure 4 is a scan taken of a 70 um copper trace in Kapton tape on an inkjet cartridge. The highlighted area is the active trace with a 100KHz signal present. This technique is comparable to CIVA, however, CIVA requires an e-beam whereas this method works in air and allows both positive and negative charge to be imposed locally for identifying floating nodes and circuit paths.

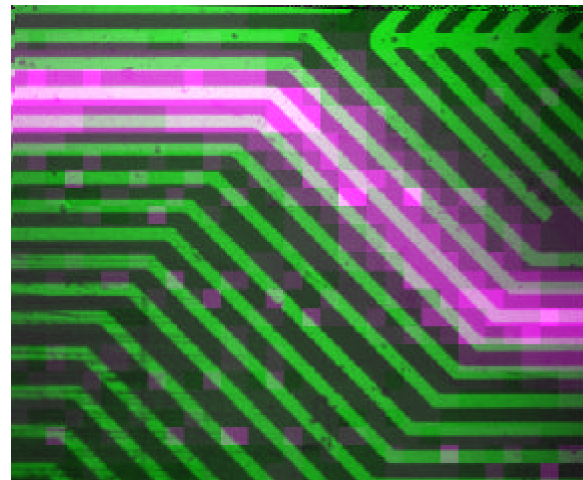


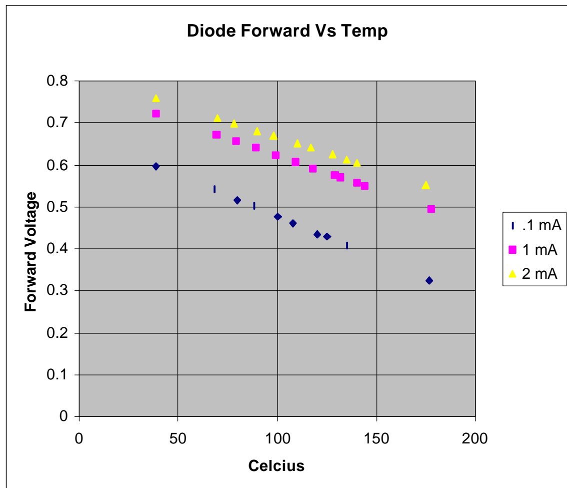
Figure 4. 70 um copper traces patterned on Kapton tape. The highlighted area is the active trace with a 100KHz signal present.

Thermal Stimulus

Thermal stimulus is useful for localizing ohmic shorts or intermittent connections as well as timing related failures. Ohmic ESD or Vdd failures are candidates for this technique. Thermal methods of SIFT scanning can be based on the following:

1. Scanning hot probe tip.
2. Laser at appropriate wavelength.
3. Magnetic Induction.

Parametric issues surrounding thermal management need to be understood so that appropriate power levels can be chosen for both frontside as well as backside analysis. A simple way to determine the required energy is to look at a diode to substrate on the device under test. Generically, the substrate diode associated with a given input pin is a known temperature sensor. Figure 5 shows the change in forward voltage for 0.1ma, 1mA, and 2mA respectively



.
Figure 5. Typical diode forward drop versus temperature relationships for 3 current drive levels.

Whereas the forward voltage may vary process to process, the ΔV can still be used to measure temperature excursions as shown in equation 1.

$$\Delta V/2.0E\text{-}3 \cong \Delta T \quad @0.1mA \qquad (1)$$
$$\Delta V/1.6E\text{-}3 \cong \Delta T \quad @1mA$$
$$\Delta V/1.5E\text{-}3 \cong \Delta T \quad @2mA$$

ΔV = Change in diode forward voltage
ΔT = Celsius change in temperature

The next parameter to evaluate is the thermal propagation in silicon for frontside and backside. For frontside, the excursion in temperature is fairly small, on the order of 5 to 10 degrees, as shown in Figure 6. Note the small fast waves are the on-off pulses of the laser and the general slope downward represents general die heating. Since the substrate is tied to a copper paddle, the general die heating is reliant on the paddle, which is floating. The temperature gradient is only 4 to 5 degrees Centigrade due to the thermal conduction of the die and paddle.

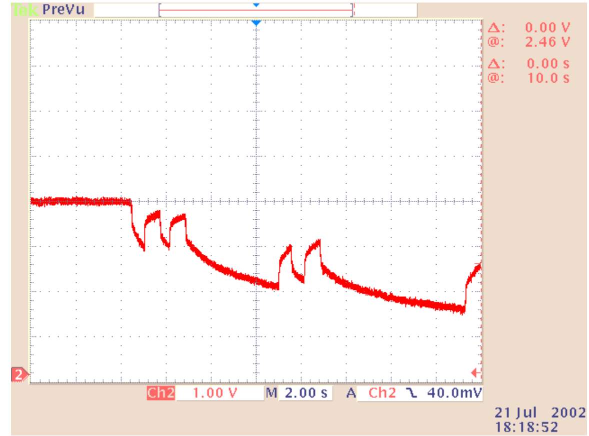


Figure 6. Thermal excursion with a pulsed IR laser on the frontside of silicon. Signal is inverted. Scale is Horz: 2 seconds/div, Vert: 5^0 C/div.

For the backside, a die was thinned to 30 um remaining silicon thickness and evaluated. Note the rapid ramp and gradient now better than 100 ^{0}C. Since the silicon is thin and has greatly reduced volume there is much less lateral heat spread.

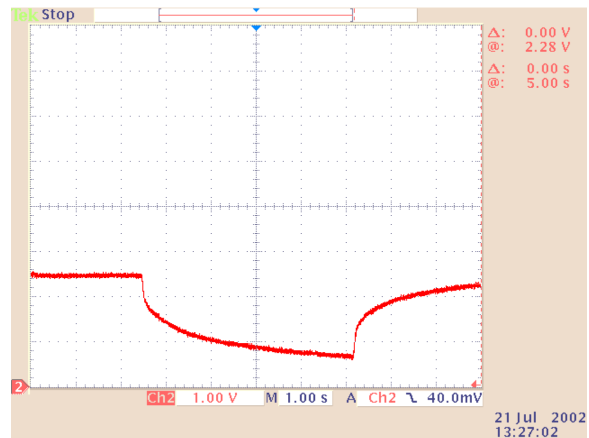


Figure 7. Thermal excursion with a pulsed IR laser on the backside of silicon. 30um thickness. Signal is inverted. Scale is Horz: 1 second/div,Vert:100 ^{0}C/div.

Thermal Stimulus using CW lasers

Normally for thermal stimulus with a laser, wavelengths outside the indirect bandgap of silicon are required, such as 1.3 um, to avoid generation of photocurrents.[11] It is difficult to get the power necessary in a large spot to heat significantly at this wavelength due to numerous factors such as laser power limitations. The silicon doesn't heat at this wavelength. The primary heating is accomplished from absorption of the laser energy by the metal, which typically scatters a significant amount of the radiation. As reported by Cole, the temperature gradient at metal is roughly 1^0C/mW with typical heating of the metal up to around 30^0C with a 1.3 um laser.[11] Temperature excursion of the related silicon

will be typically less than 1^{0}C, inadequate for silicon based thermal analyses.

Functional SIFT needs to be able to scan a large spot with sufficient energy to create thermal gradients in the silicon as well as metal. The scan area and laser spot size are successively reduced, based on results, so the math doesn't become a problem. If the tester can loop every 100 msec and the spot size is 1 um across a small die such as 2mmX2mm it will take 400000 seconds (4.6 days) to complete 1 scan. SIFT allows for variable spot sizes and step values to allow quick reduction of the scan area to minutes. SIFT also needs to create a significant temperature gradient in order to differentiate functional timing failures.

Ordinarily, shorter wavelength lasers generate too much photocurrent to be useful thermally. Several laser wavelengths of importance, due to their ability to generate higher power, are: 532nm, 808nm, 940nm, and 1064nm. All of these wavelengths will generate photocurrents unless they are masked from the die. This is accomplished by applying high temperature flat black paint to the die surface by spray, brush or spin deposition. The 532nm laser does not need to be masked when used backside due to the absorption of the laser by the silicon substrate. Carbon sputtering can also be used backside or frontside if the connections are passivated first. A 5 watt 808nm laser was chosen to locally heat the surface with around 1 to 2 watts depending on spot size and desired heating. No photocurrents are generated, as shown in figures 8 and 9, due to the opaque layer.

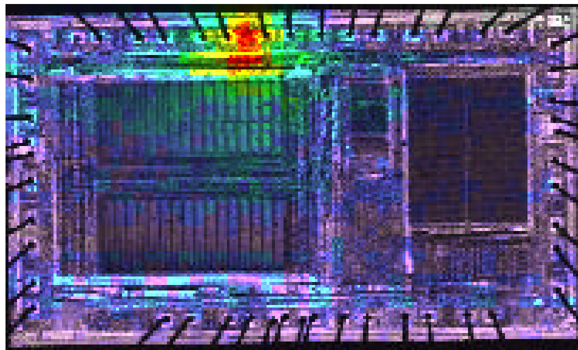


Figure 8. Frontside 808nm-laser thermal SIFT scan of an input diode. The hot zone is in red and represents a 5 ^{0}C rise locally at the monitor diode. Spot size is 1 mm.

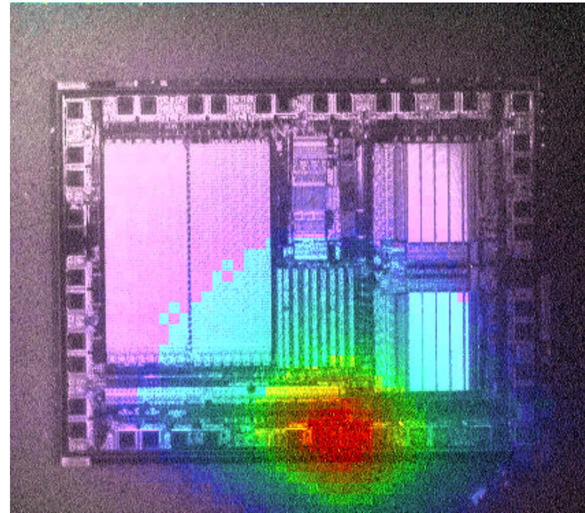


Figure 9. Backside 808nm laser thermal SIFT scan of an input diode. The hot zone is in red and represents a 100 ^{0}C rise locally at the monitor diode. Silicon thickness is 30 um. Laser spot size is 1 mm.

High Frequency Magnetic Induction

By scanning a miniature induction coil over the device, as shown in figure 10, package level shorts can be mapped. The spatial resolution is currently limited to about 2 mm based on the frequency used (10-20 MHz). Magnetic induction couples and directly heats the conductors embedded in a package due to formed eddy currents within the IC. The device can be operated during the scan and multilayer devices are well suited for induction based on coupling. The power supply was developed for this application, as commercial units cannot operate at these high frequencies. Parametric shifts of the diode in the corner of figure 11 are monitored during the scan by the microcontroller in relation to the coordinates. Induction also allows monitoring of phase based on coupling to the conductors. Imaging is possible due to phase/frequency relationships during the scan. Future work is intended at higher frequencies to address these possibilities but is beyond the scope of this paper.

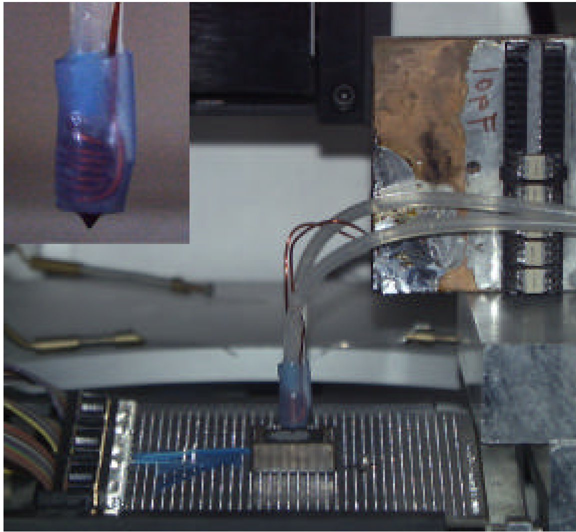


Figure 10. Induction heat probe set up over the die. Close up view of the tip is offset in the upper left corner.

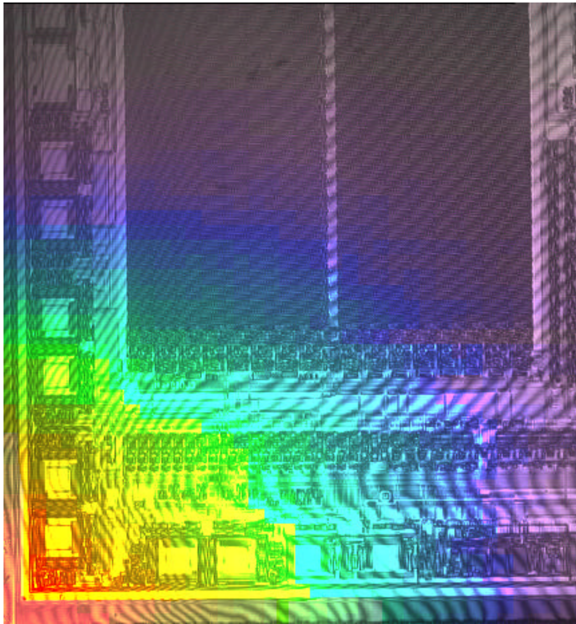


Figure 11. Induction heat scan over an IC at 16.2 MHz from the backside.

Functional SIFT

Now that the foundations have been laid, the pieces of the puzzle come together as functional SIFT. Functional SIFT is based on pass/fail test criteria that can be complete vector tests including parametrics or subsets as appropriate. The setup involves a quick interface to a tester display with photosensors, such as shown in figure 12, or direct wiring to the tester. The photosensors are attached to the LCD screen with double stick tape at the appropriate locations on the screen. The clear advantage to this method is that the tester can be of any type allowing multiple links to the SIFT scanner without any tester modification.

The simplest method is to monitor the pass-fail light bar on a tester and strobe the SIFT through full test loops. This allows the die to be fully tested at each stimulus coordinate controlled by the SIFT scanner. In the case of figure 12, two sensors are used. The sensor labeled D is the data sensor, which looks for a change in data after sensor S transitions from low to high (strobe). After a strobe, the scanner will move to the next coordinate in the scan. It may sound complicated, but it actually boils down to looping the test program, (even if it was written by someone who left the company years ago) setting the spot size and intensity to trigger the failure and running the scan. Obviously, the sensors can monitor presence or absence of numeric data or pass fail flags on the screen as needed. Multiple sensors can be used to overlay several data parameters at the same time. Future work will involve direct connection to the tester video interface.

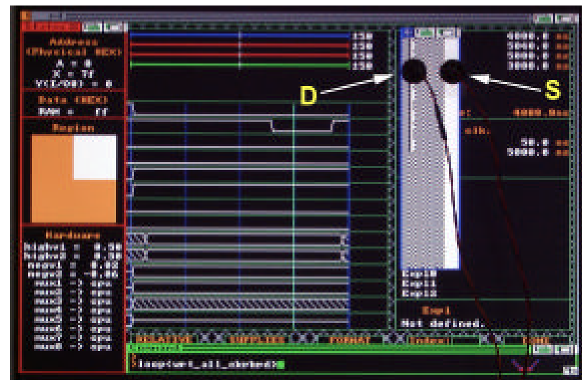


Figure 12. View of the screen on a tester with 2 sensors affixed. The sensor labeled D is the data sensor, which looks for a change in data after sensor S transitions from low to high (strobe).

A die scan over the entire die using a 670nm laser was performed to identify a faulty Y decoder causing several SRAM columns to fail. Light sensitivity of the die was noted. SIFT was used linked to the tester with the laser spot set to .5mm and the scanner set to .4mm to allow overlap of the 2.9X5.1mm die. The scan size in pixels, with plenty of die overlap, was 9X14 equating to 126 test loops to complete the die scan. The loop was 1 second requiring 126 seconds to scan the entire die. Although images are being provided to show the location, the scanner actually gives exacting coordinates for each sample point. In this case, 126 coordinates were output with associated sensor readings. This allows for linking to CAD layout. Figures 14 and 15 are reduced area scans where the spot was also scaled down. Each scan took <5 minutes to complete.

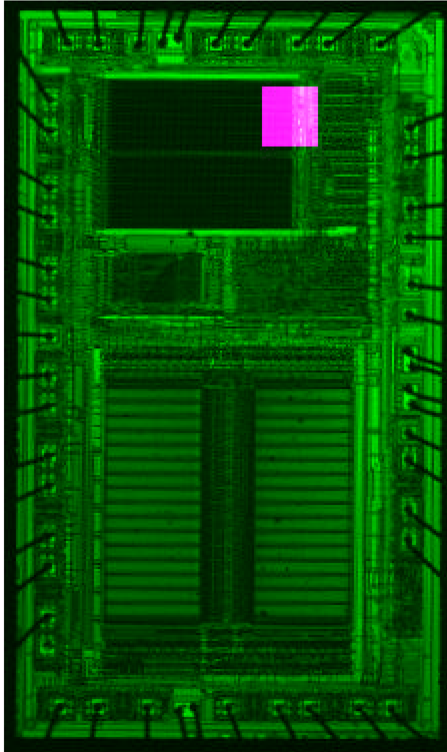


Figure 13. Full die scan showing fault node at coordinates 1853,4375 um using a 500 um spot size.

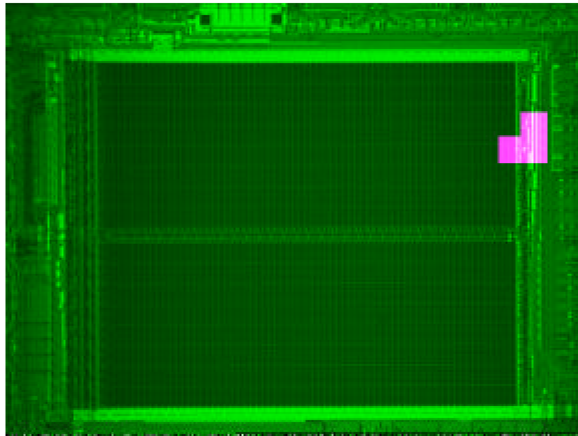


Figure 14. Reduced area scan showing the fault node area with 100um spot size.

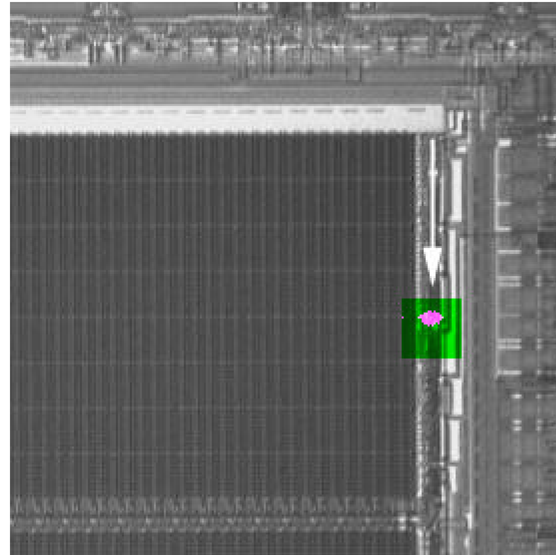


Figure 15. SIFT Scan showing exact location of fault node in Y decoder at X=1815um Y=4334um.
The green square is the active scan area with magenta areas the fault signal.

Summary

A new method of complete failure analysis has been presented which now allows multiple beam based stimulus to be linked to any tester or parametric analyzer. The problem of insufficient laser power and insufficient thermal gradients to analyze functional failures has been overcome with backside preparation as well as mask methods. 100^{0}C temperature gradients are now routine, allowing timing sensitive failures to be localized as well as a host of failure mechanisms. SIFT techniques have been shown for both traditional laser based techniques as well as new methods. Comparative disturb between reference and failing or threshold dependent failures is now possible. Variable spot size allows faster scans and uniform stimulus of larger blocks on an IC for timing/thermal analyses. Stimulus includes thermal, high frequency magnetic induction, OBIC and RF injection using a scanning probe tip. Since the data is based on coordinate information, it can be converted to the traditional photo form or analyzed for maxima and minima based on coordinates for x and y in spreadsheet form as well as CAD overlays. Scan size is virtually unlimited. Scan speed is limited both by stepper speed and loop test time.

Acknowledgments

To my wife Mayra for her devotion and patience with my burning the candle at both ends.

References

1. E.I. Cole, P. Tangyunyong, CF Hawkins, MR Bruce, VJ Bruce, RM Ring, WL Chong " Resistive Interconnect Localization" ISTFA 2001 pp. 43-50.
2. Reports 6-4745,7-E0019, 7-M0278, 7-E0051, and 7-M0462 Delco Electronics Failure Analysis Reports by Jim Colvin 1986-1987.
3. B. Bossmann, et al., "Failure Analysis Techniques with the Confocal Laser Scanning Microscope", ISTFA/92 Proceedings, pp. 351-361.
4. E.I. Cole Jr., J.M. Soden, J.L. Rife, D.L. Barton, and C.L. Henderson, "Novel Failure Analysis Techniques Using Photon Probing in a Scanning Optical Microscope", IRPS, 1994, pp. 388-398.
5. E.I. Cole Jr., P. Tangyunyong, D.L. Barton, "Backside Localization of Open and Shorted IC Interconnections", IRPS, 1998, pp. 129-136.
6. E.I. Cole et al" TIVA and SEI Developments for Enhanced Front and Backside Interconnection Failure Analysis" European Symp. On Reliability of Electron Devices (ESREF), pp. 991-996, Oct. 1999.
7. K. Nikawa and S. Inoue, " New Capabilities of OBIRCH Method for Fault Localization and Defect Detection" Proc. 6th Asian Test Symp., p. 219, July 1997.
8. R. Aaron Falk,"Advanced LIVA/TIVA Techniques" ISTFA/2001 Proceedings, pp. 59-65.
9. Ibid, pp. 59-65.
10. J. Colvin,"The Identification of Compromised Oxide Interfaces Using Noise Signature Techniques From a Constant Current Source" ISTFA/1994 Proceedings, pp. 1-8.
11. U.S. Patent # 6,078,183 "Thermally-induced voltage alteration for integrated circuit analysis," Cole, Jr.; Edward I. Sandia Corporation (Albuquerque, NM)